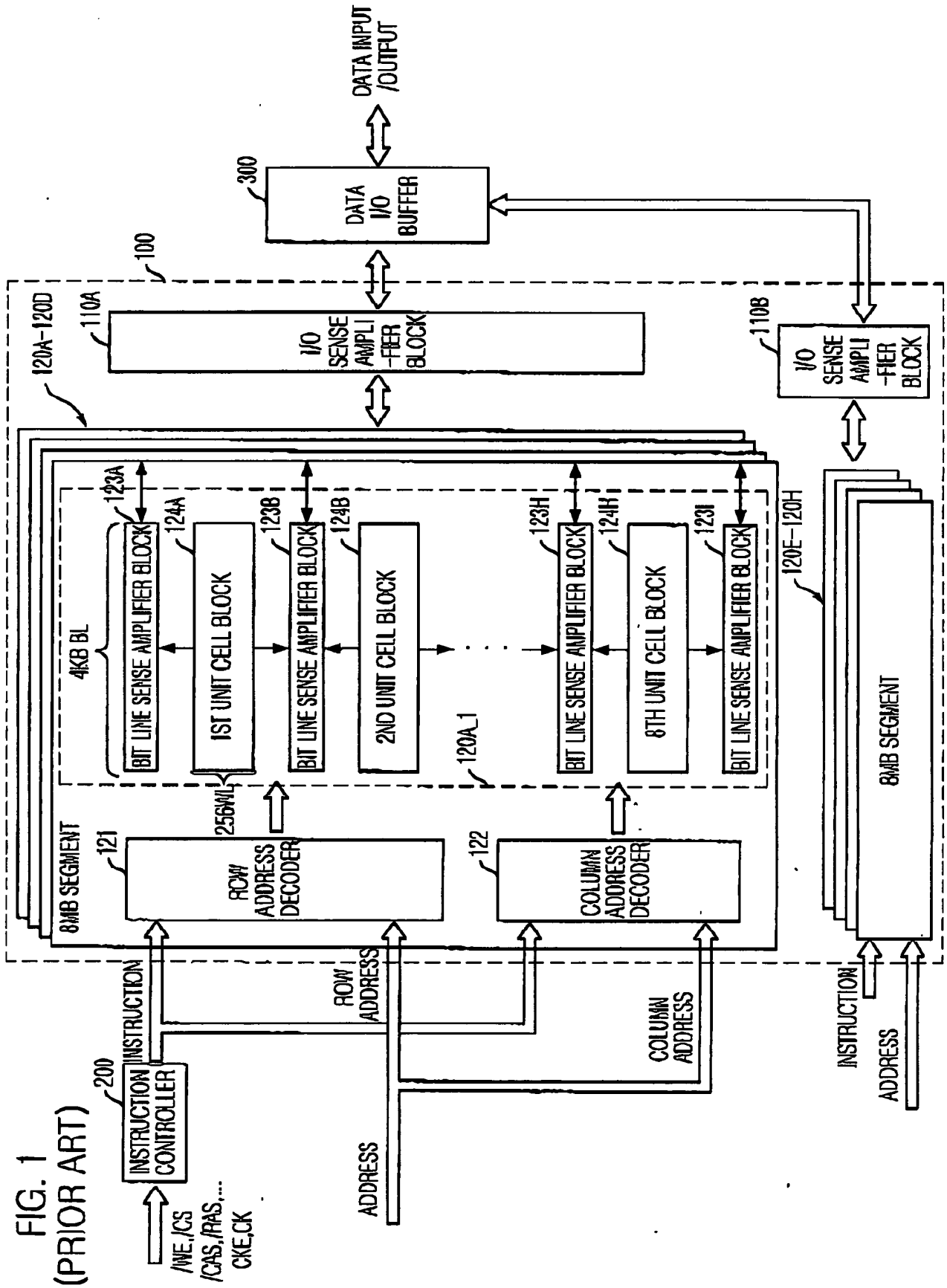


FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

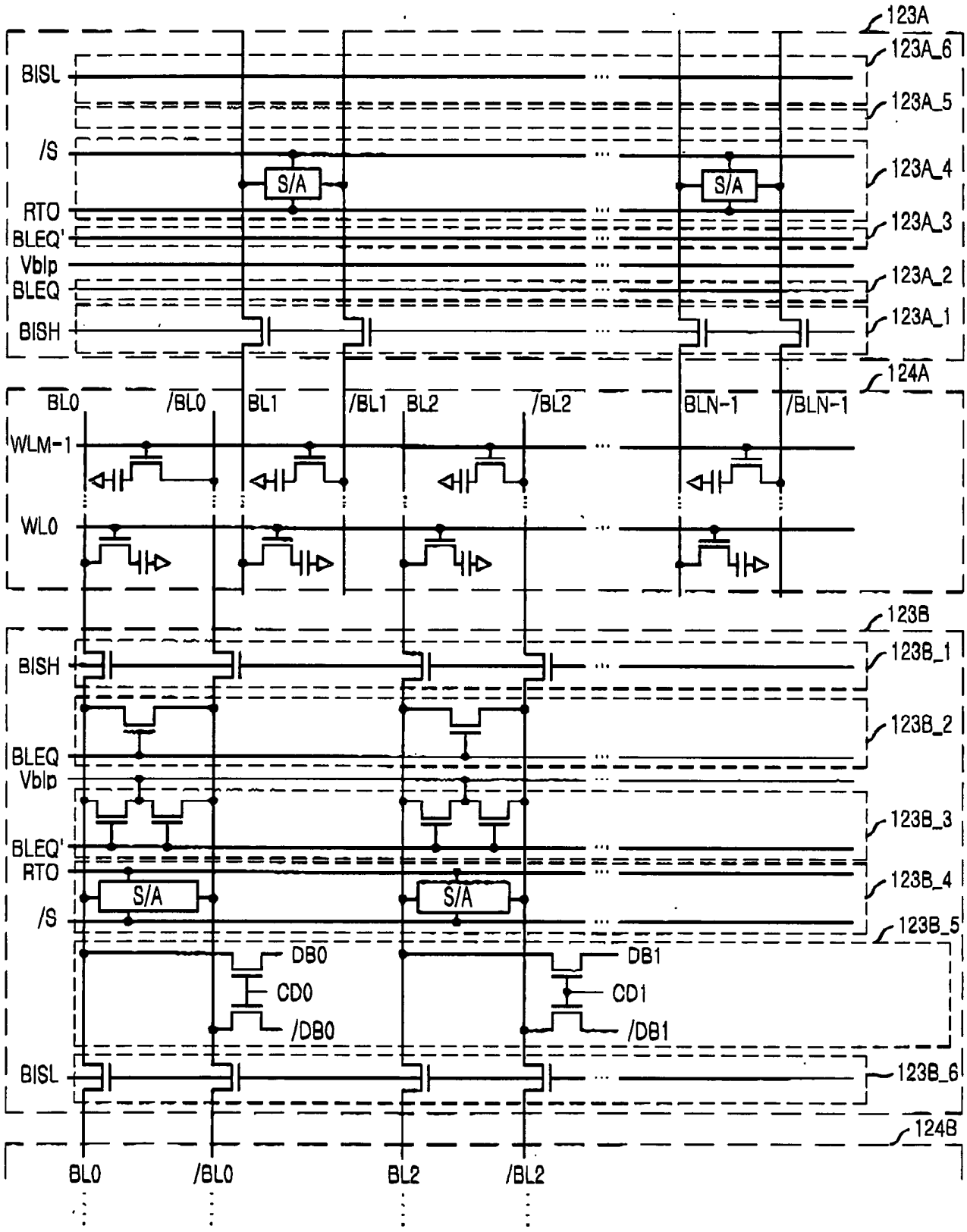


FIG. 3
(PRIOR ART)

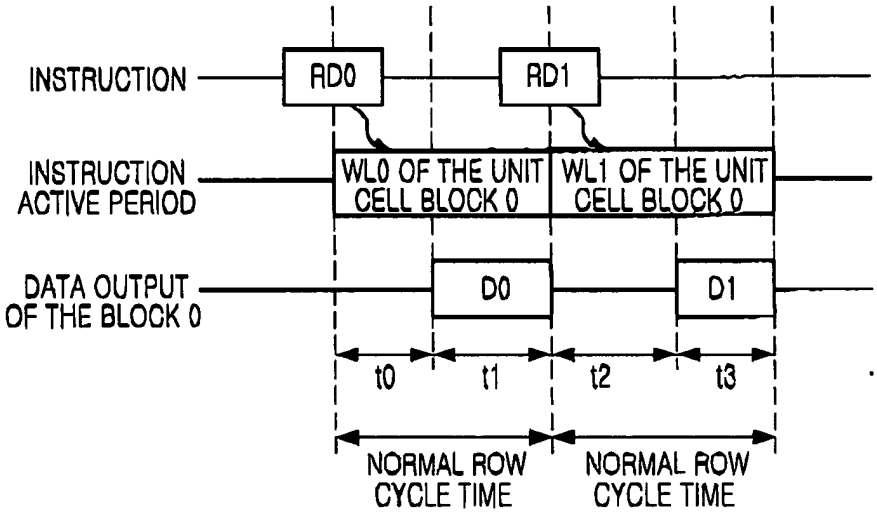


FIG. 4
(PRIOR ART)

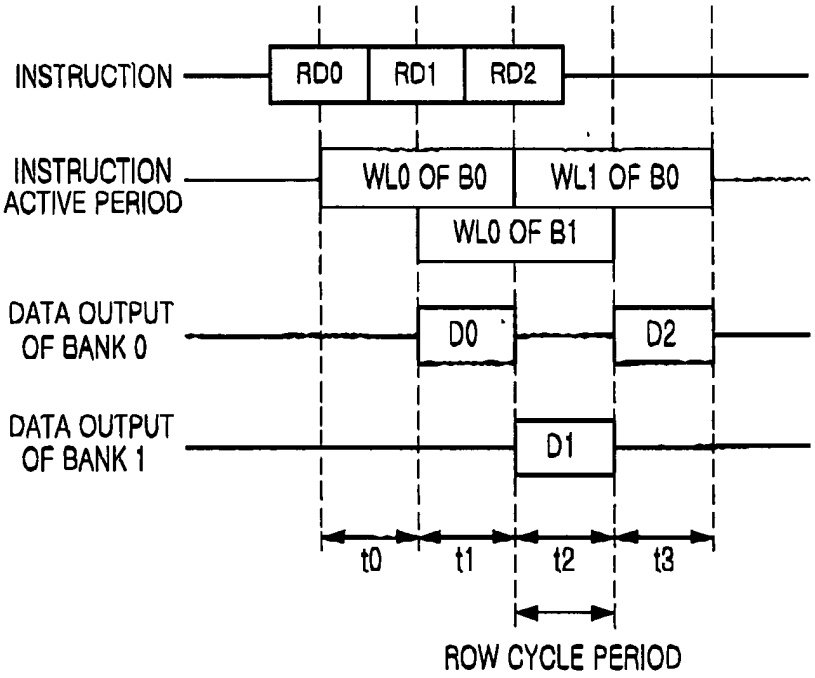


FIG. 5

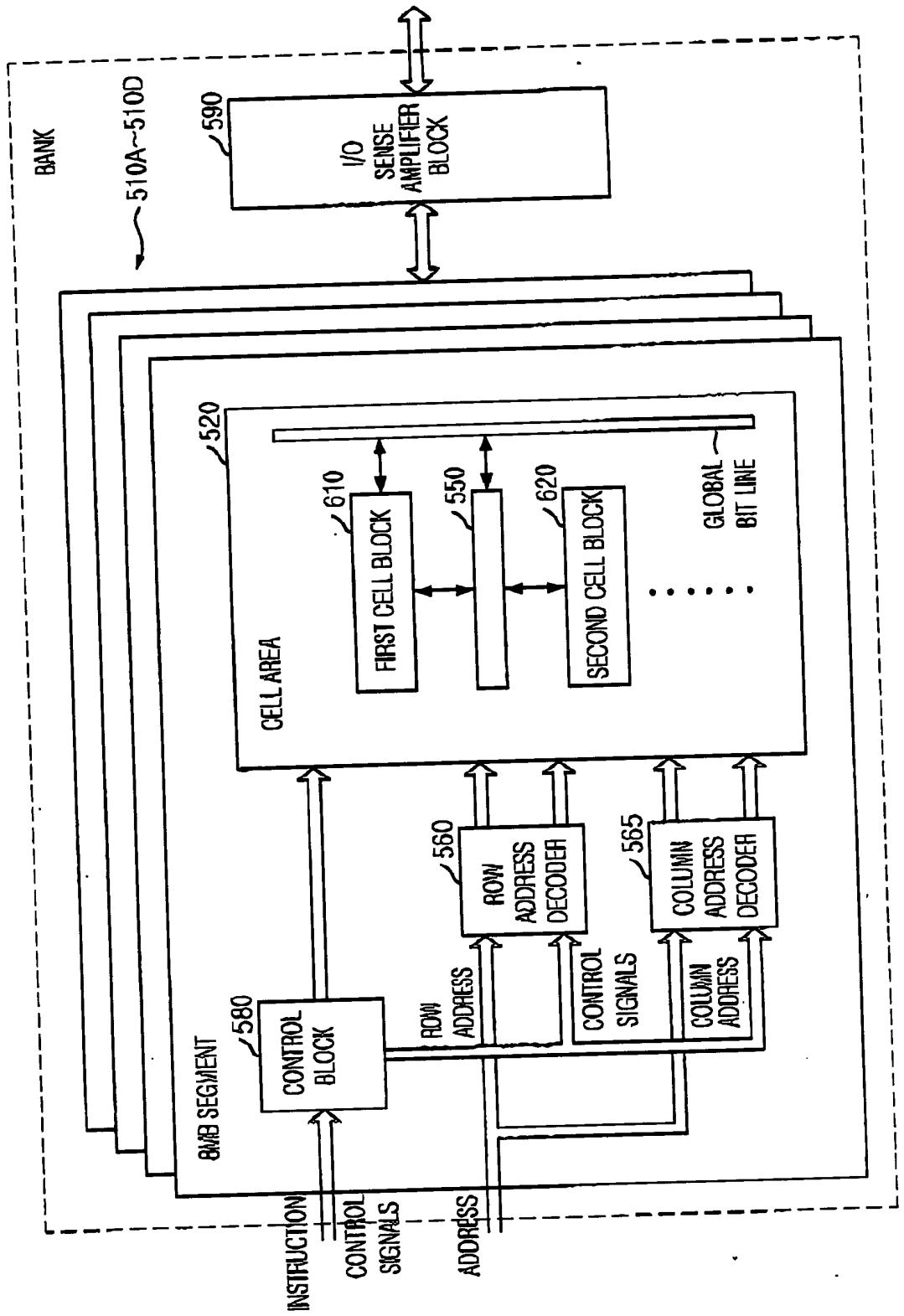

BANK
510A~510D
590
I/O SENSE AMPLIFIER BLOCK
520
610
FIRST CELL BLOCK
550
620
SECOND CELL BLOCK
GLOBAL BIT LINE
CELL AREA
560
ROW ADDRESS DECODER
565
COLUMN ADDRESS DECODER
8MB SEGMENT
580
CONTROL BLOCK
ROW ADDRESS
CONTROL SIGNALS
COLUMN ADDRESS
INSTRUCTION
CONTROL SIGNALS
ADDRESS

FIG. 6

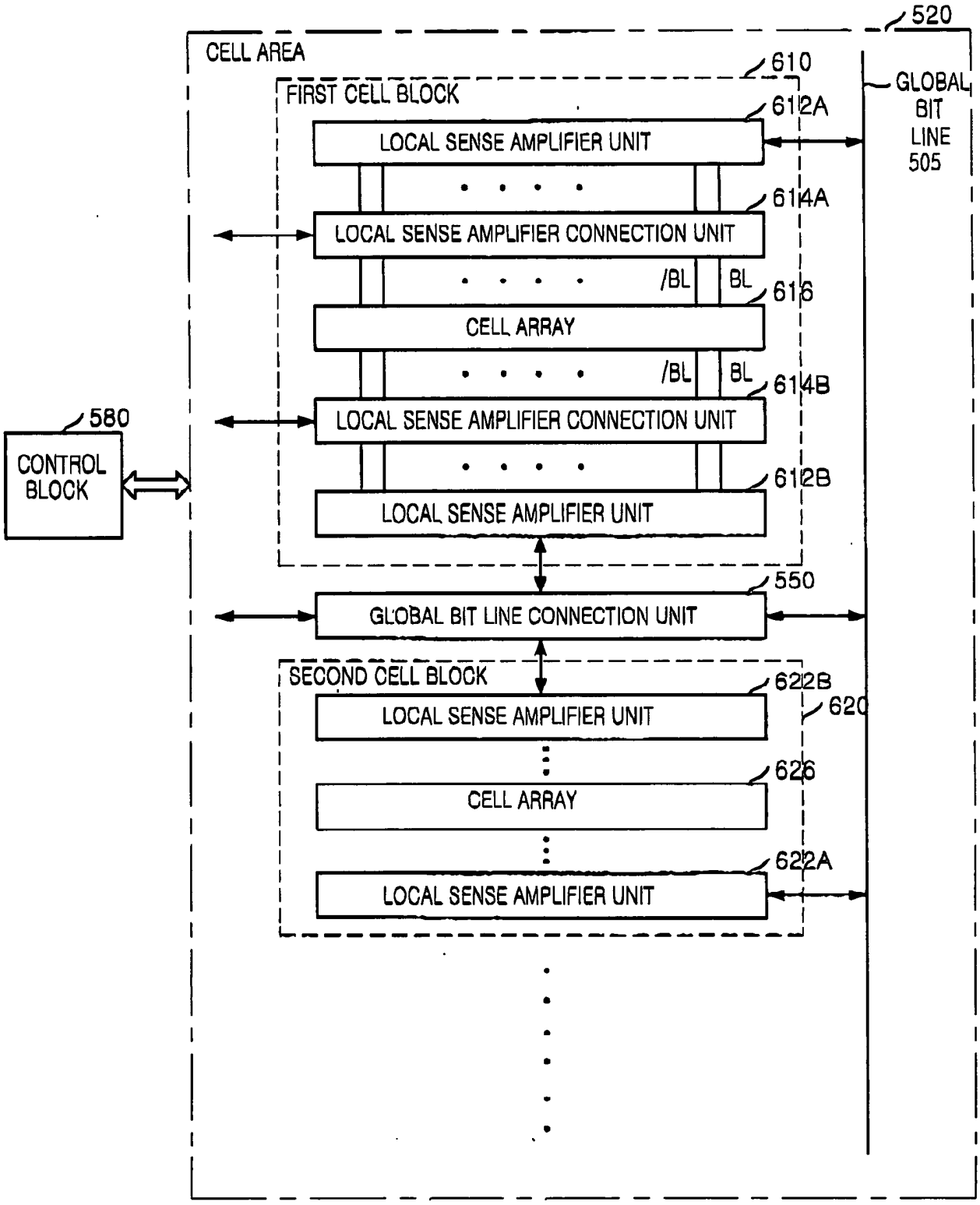

520
CELL AREA
610
FIRST CELL BLOCK
612A
LOCAL SENSE AMPLIFIER UNIT
GLOBAL BIT LINE 505
614A
LOCAL SENSE AMPLIFIER CONNECTION UNIT
/BL
BL
616
CELL ARRAY
/BL
BL
614B
LOCAL SENSE AMPLIFIER CONNECTION UNIT
580
CONTROL BLOCK
612B
LOCAL SENSE AMPLIFIER UNIT
550
GLOBAL BIT LINE CONNECTION UNIT
SECOND CELL BLOCK
622B
620
LOCAL SENSE AMPLIFIER UNIT
626
CELL ARRAY
622A
LOCAL SENSE AMPLIFIER UNIT

FIG. 7

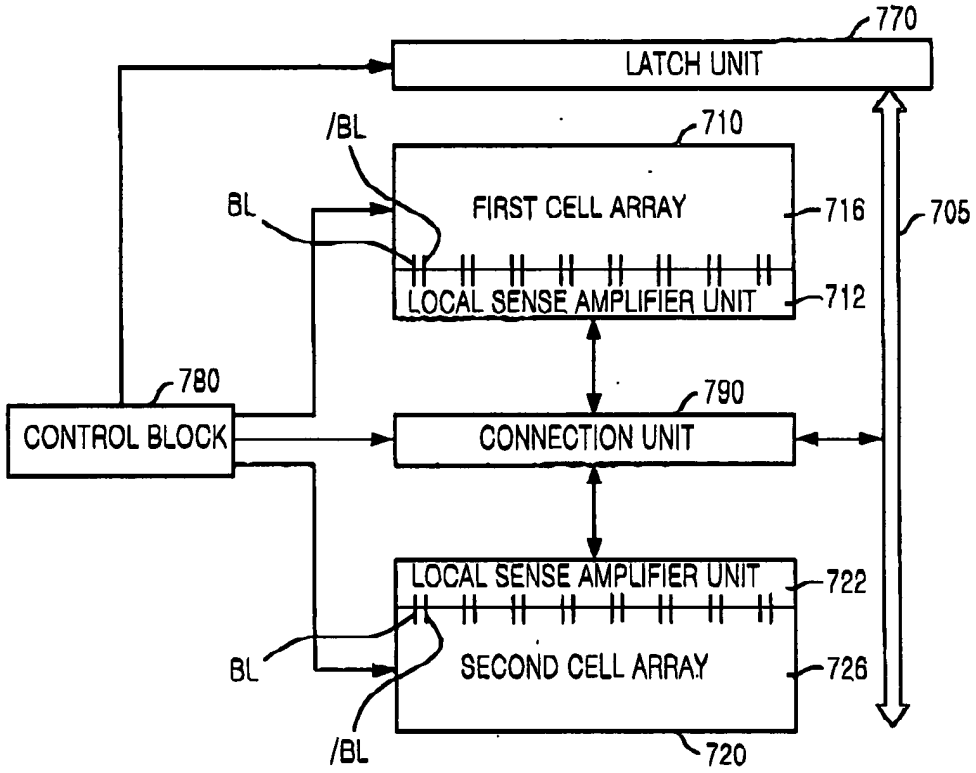

770
LATCH UNIT
/BL
710
BL
FIRST CELL ARRAY
716
705
LOCAL SENSE AMPLIFIER UNIT
712
780
790
CONTROL BLOCK
CONNECTION UNIT
LOCAL SENSE AMPLIFIER UNIT
722
BL
SECOND CELL ARRAY
726
/BL
720

FIG. 8

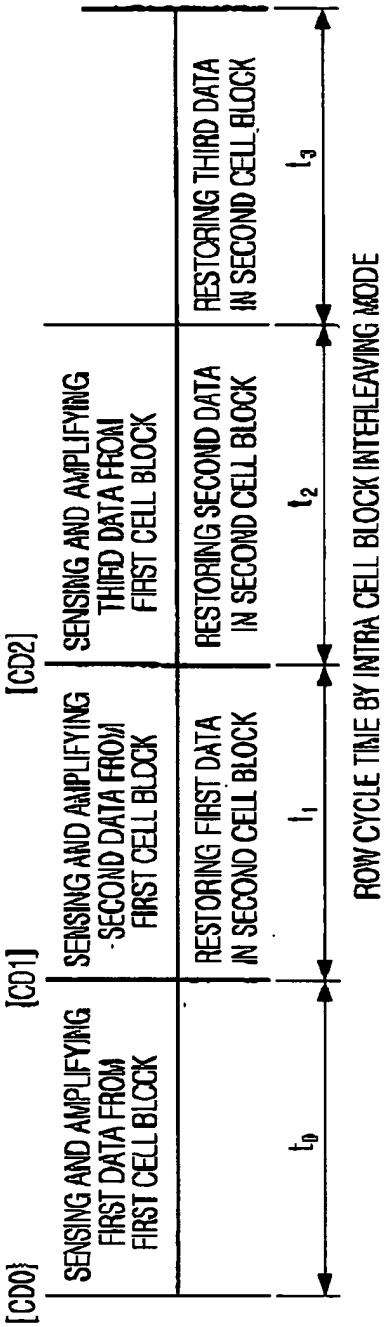

[CD0]
[CD1]
[CD2]
SENSING AND AMPLIFYING FIRST DATA FROM FIRST CELL BLOCK
SENSING AND AMPLIFYING SECOND DATA FROM FIRST CELL BLOCK
RESTORING FIRST DATA IN SECOND CELL BLOCK
SENSING AND AMPLIFYING THIRD DATA FROM FIRST CELL BLOCK
RESTORING SECOND DATA IN SECOND CELL BLOCK
RESTORING THIRD DATA IN SECOND CELL BLOCK
t_0
t_1
t_2
t_3
ROW CYCLE TIME BY INTRA CELL BLOCK INTERLEAVING MODE
< INTRA CELL BLOCK DATA ACCESS>

FIG. 9

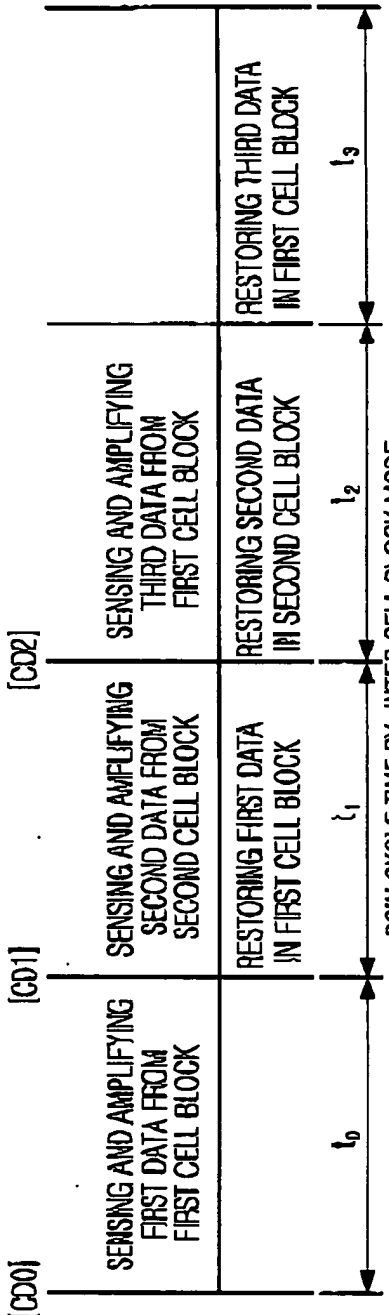
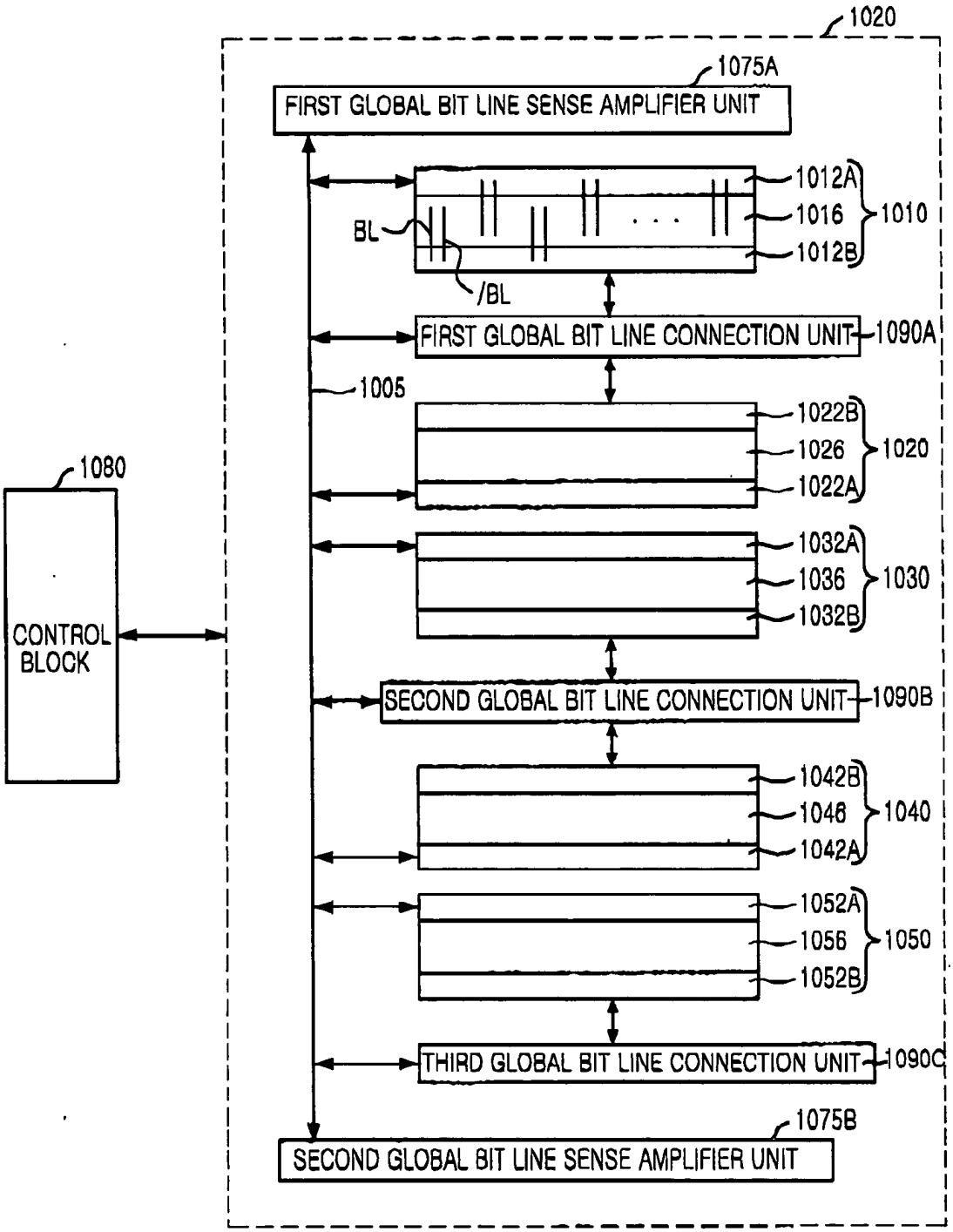

[CD0]
[CD1]
[CD2]
SENSING AND AMPLIFYING FIRST DATA FROM FIRST CELL BLOCK
SENSING AND AMPLIFYING SECOND DATA FROM SECOND CELL BLOCK
SENSING AND AMPLIFYING THIRD DATA FROM FIRST CELL BLOCK
RESTORING FIRST DATA IN FIRST CELL BLOCK
RESTORING SECOND DATA IN SECOND CELL BLOCK
RESTORING THIRD DATA IN FIRST CELL BLOCK
t_0
t_1
t_2
t_3
ROW CYCLE TIME BY INTERLEAVING AMONG CELL BLOCKS
INTER CELL BLOCK MODE
< INTER CELL BLOCK DATA ACCESS>

FIG. 10


1020
1075A
FIRST GLOBAL BIT LINE SENSE AMPLIFIER UNIT
1012A
1016
1012B
1010
BL
/BL
FIRST GLOBAL BIT LINE CONNECTION UNIT
1090A
1005
1022B
1026
1022A
1020
1080
CONTROL BLOCK
1032A
1036
1032B
1030
SECOND GLOBAL BIT LINE CONNECTION UNIT
1090B
1042B
1046
1042A
1040
1052A
1056
1052B
1050
THIRD GLOBAL BIT LINE CONNECTION UNIT
1090C
1075B
SECOND GLOBAL BIT LINE SENSE AMPLIFIER UNIT

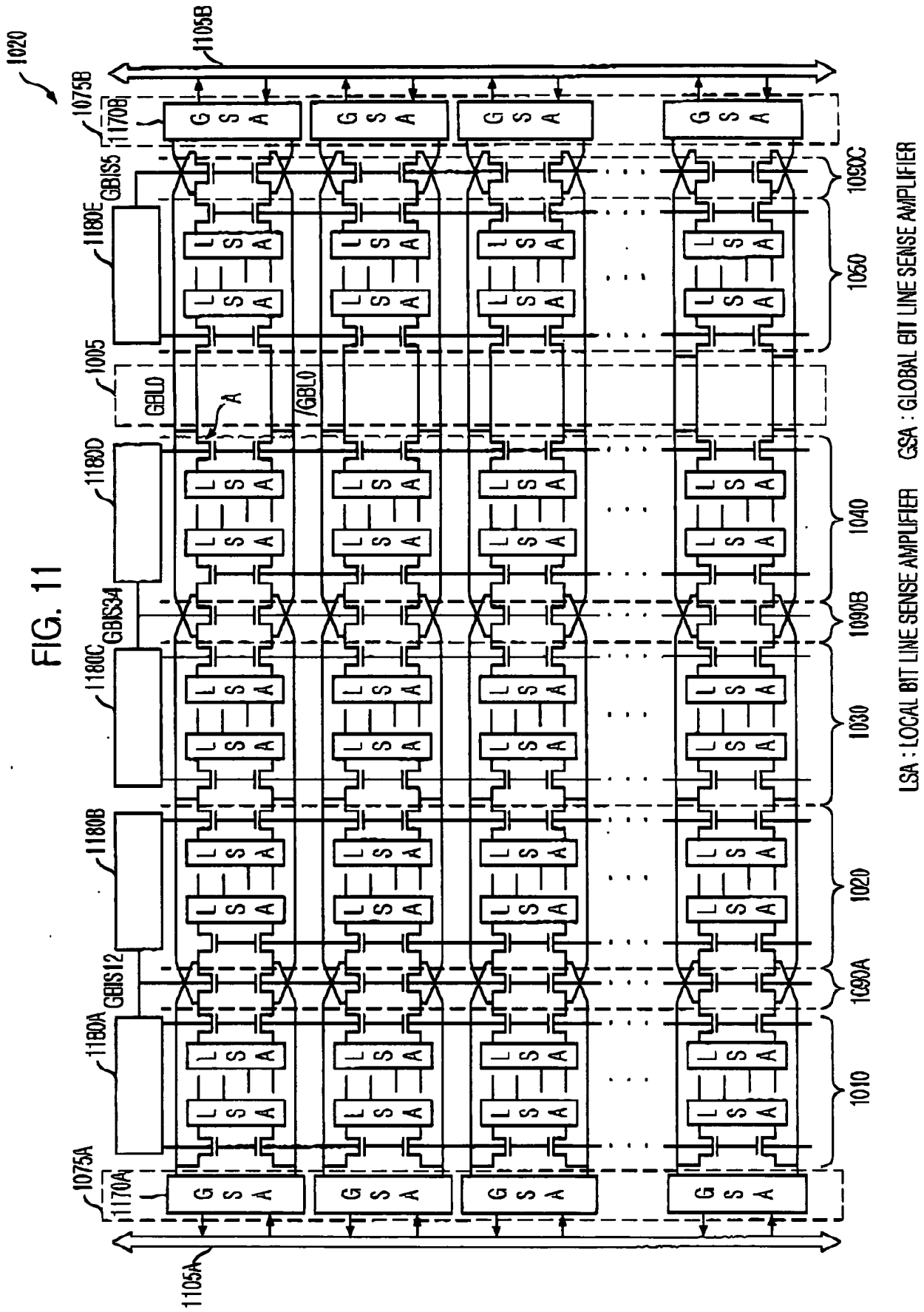

1020
1105B
1075B
1170B
GBIS5
1180E
1005
GBLO
/GBLO
1180D
GBIS34
1180C
1180B
GBIS12
1180A
1075A
1170A
1105A
1090C
1050
1040
1090B
1030
1020
1090A
1010
G S A
L S A
LSA : LOCAL BIT LINE SENSE AMPLIFIER
GSA : GLOBAL BIT LINE SENSE AMPLIFIER

FIG. 11

FIG. 12

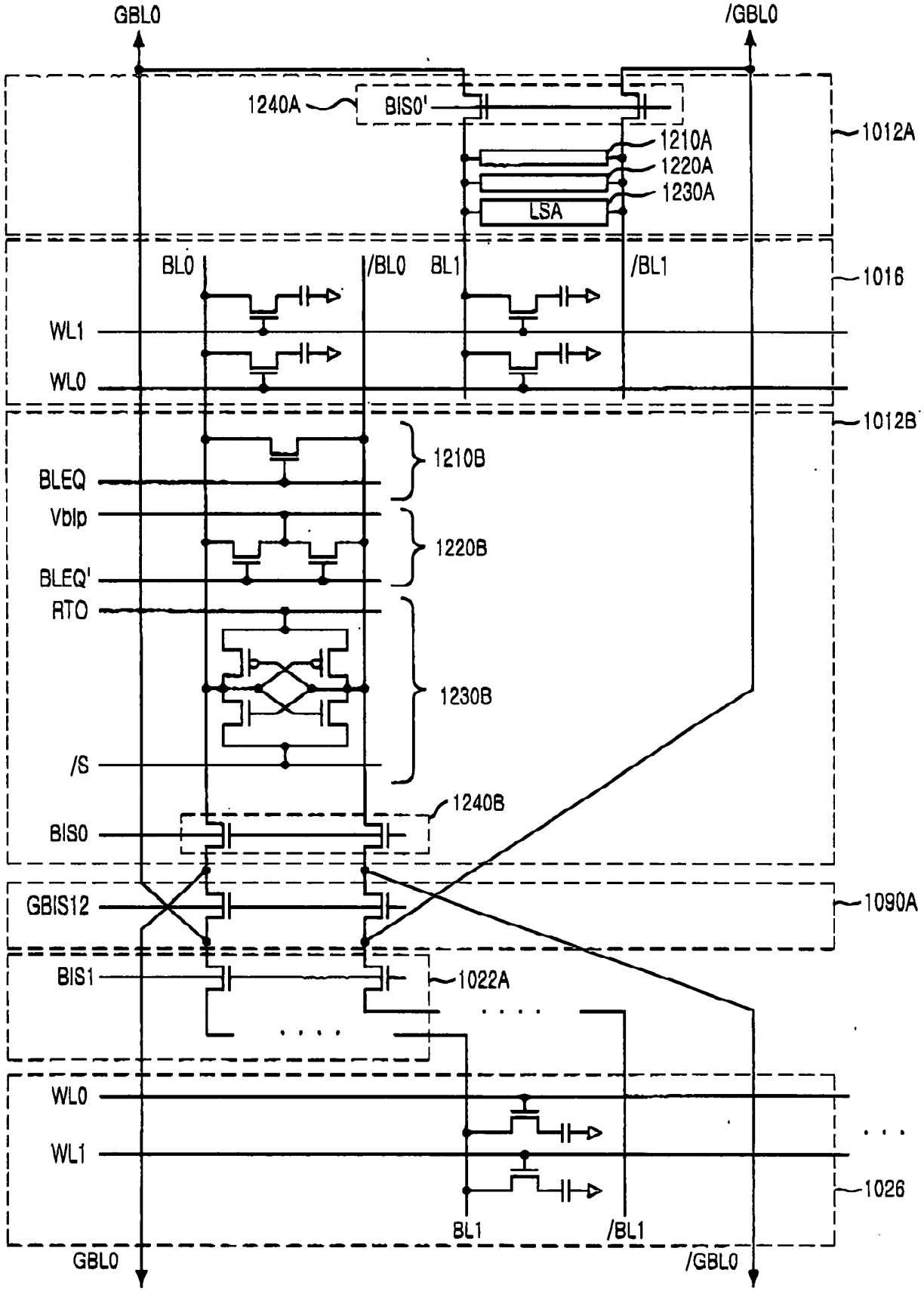

GBL0
/GBL0
1240A
BIS0'
1012A
1210A
1220A
1230A
LSA
BL0
/BL0
BL1
/BL1
1016
WL1
WL0
1012B
1210B
BLEQ
Vblp
1220B
BLEQ'
RTO
1230B
/S
1240B
BIS0
GBIS12
1090A
BIS1
1022A
WL0
WL1
1026
BL1
/BL1
GBL0
/GBL0

FIG. 13A

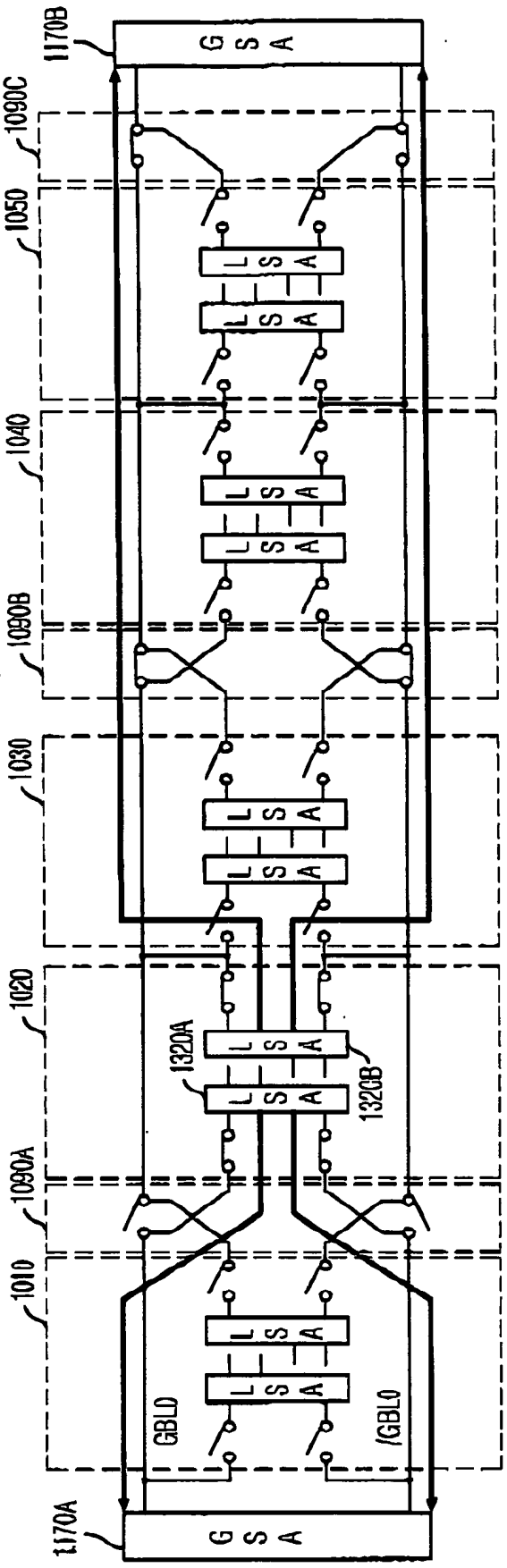

1170B
G S A
1090C
1050
L S A
1040
1090B
1030
1020
1320A
1320B
1090A
1010
GBL0
/GBL0
1170A

FIG. 13B

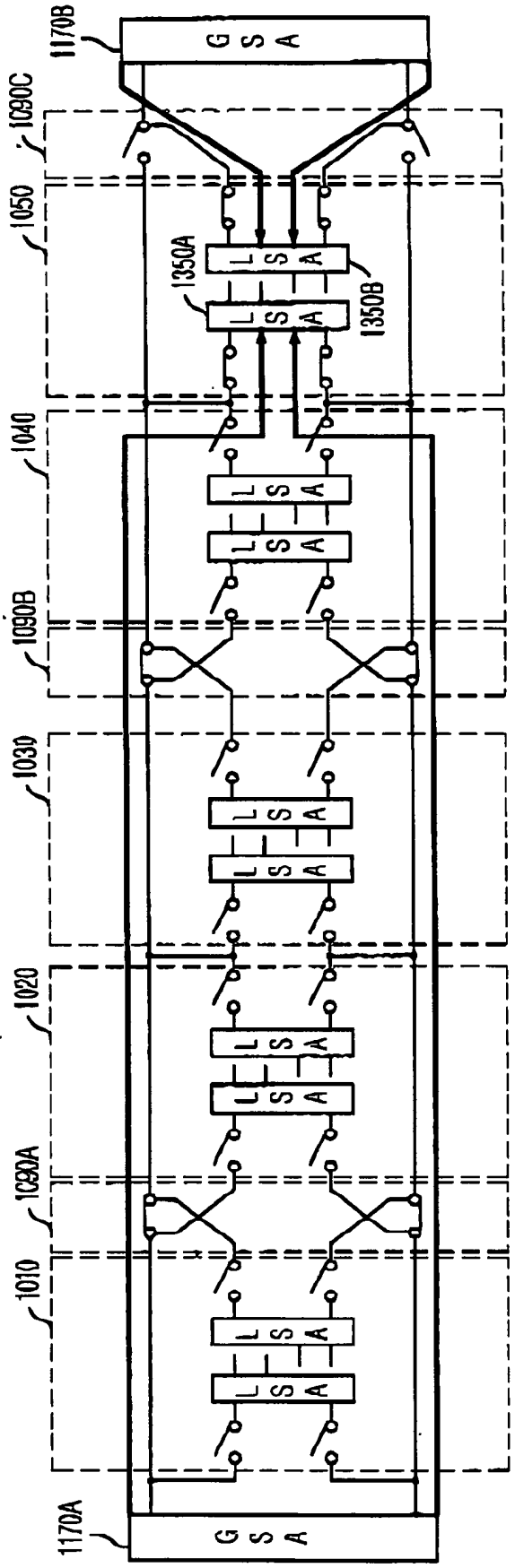

1170B
G S A
1090C
1050
1350A
1350B
L S A
1040
1090B
1030
1020
1090A
1010
1170A

FIG. 13C

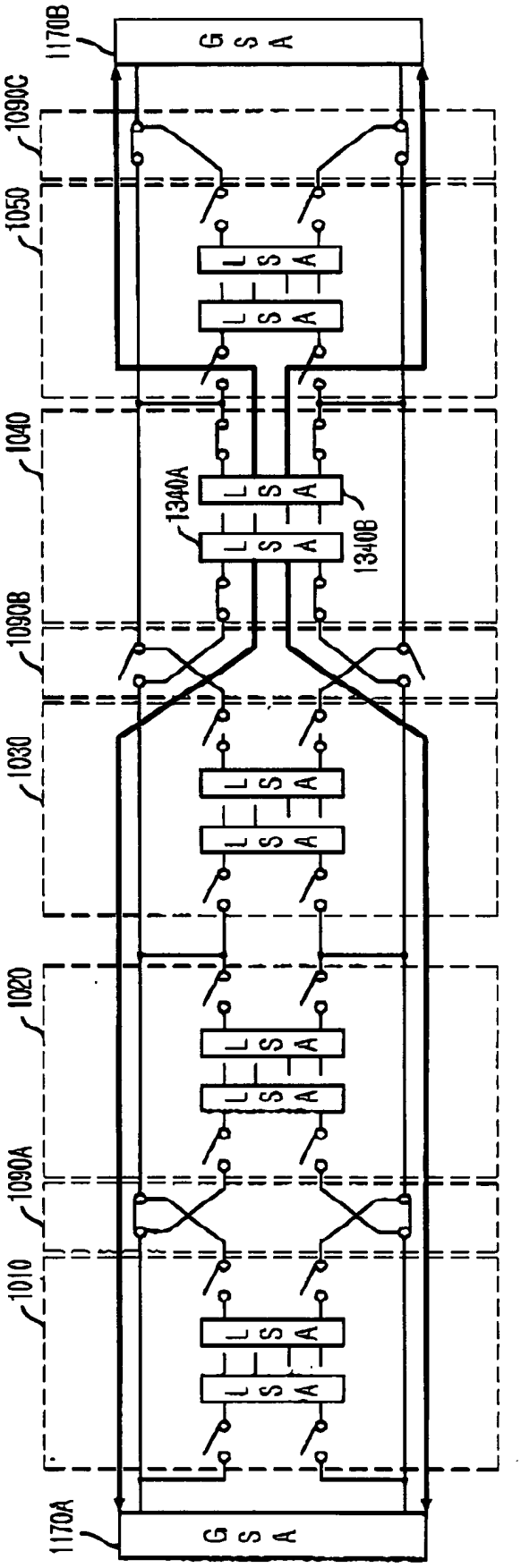

1170B
G S A
1090C
1050
L S A
L S A
1040
1340A
L S A
1340B
L S A
1090B
1030
L S A
L S A
1020
L S A
L S A
1090A
1010
L S A
L S A
1170A
G S A

FIG. 13D

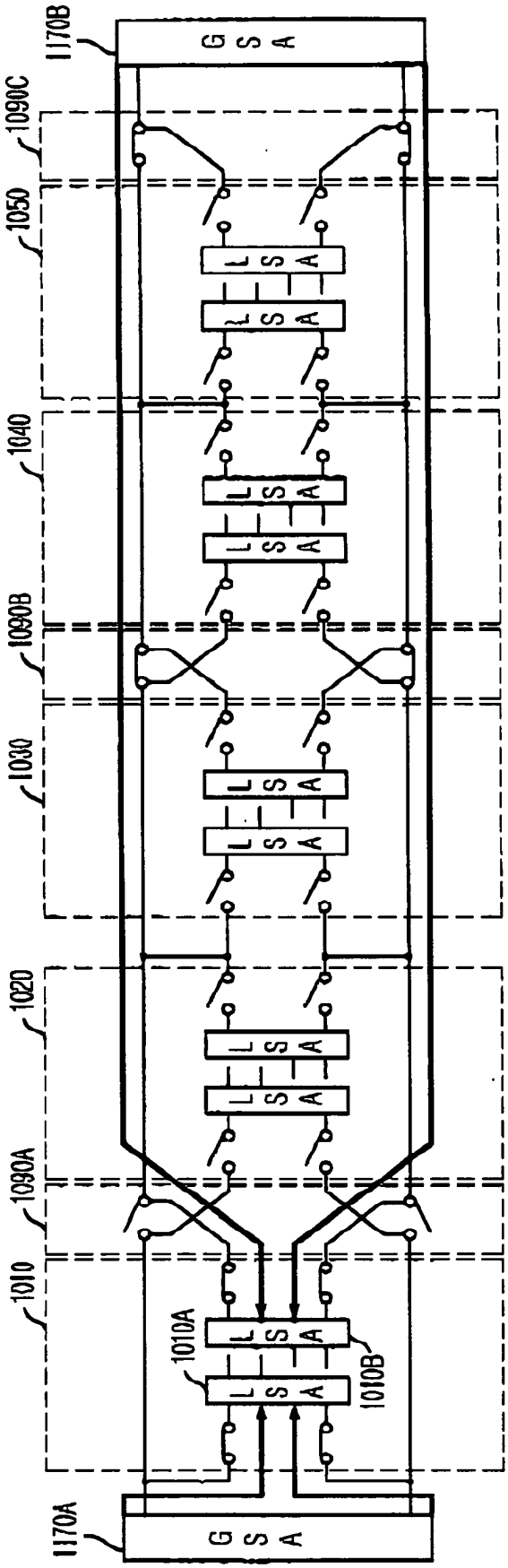

1170B
G S A
1090C
1050
L S A
1040
1090B
1030
1020
1090A
1010
1010A
1010B
1170A

FIG. 14

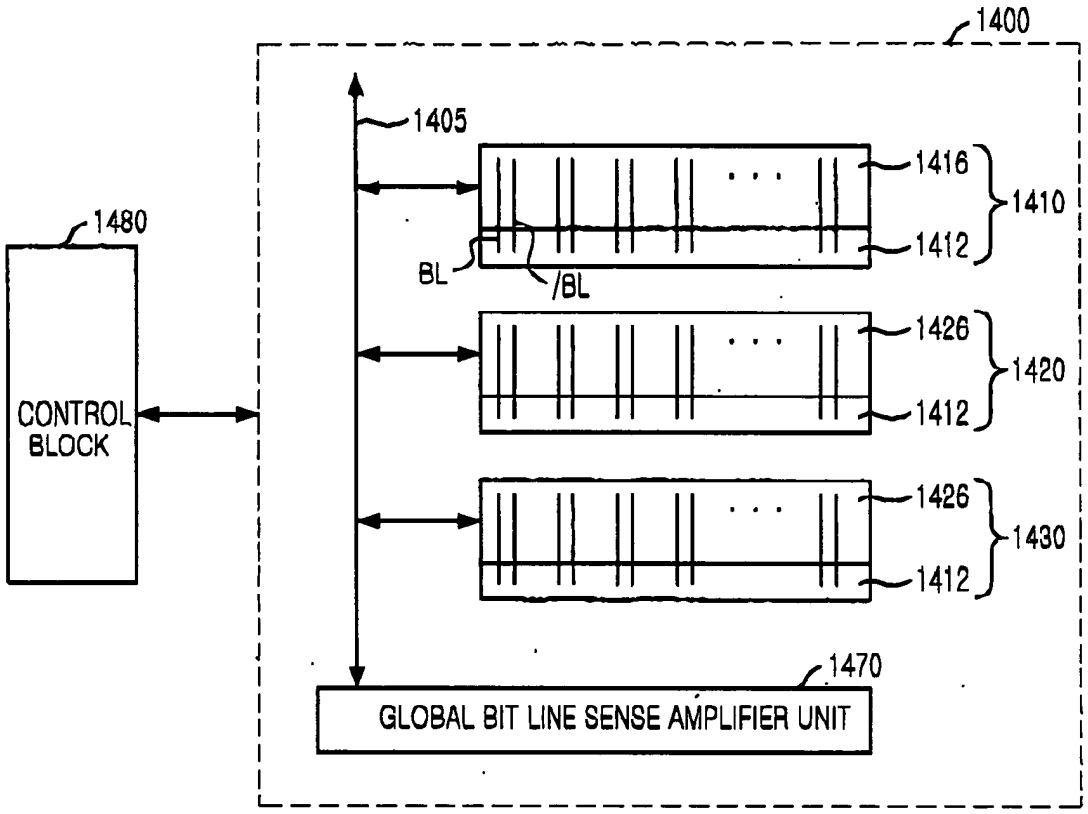

1400
1405
1480
CONTROL BLOCK
1416
1412
1410
BL
/BL
1426
1412
1420
1426
1412
1430
1470
GLOBAL BIT LINE SENSE AMPLIFIER UNIT

FIG. 15

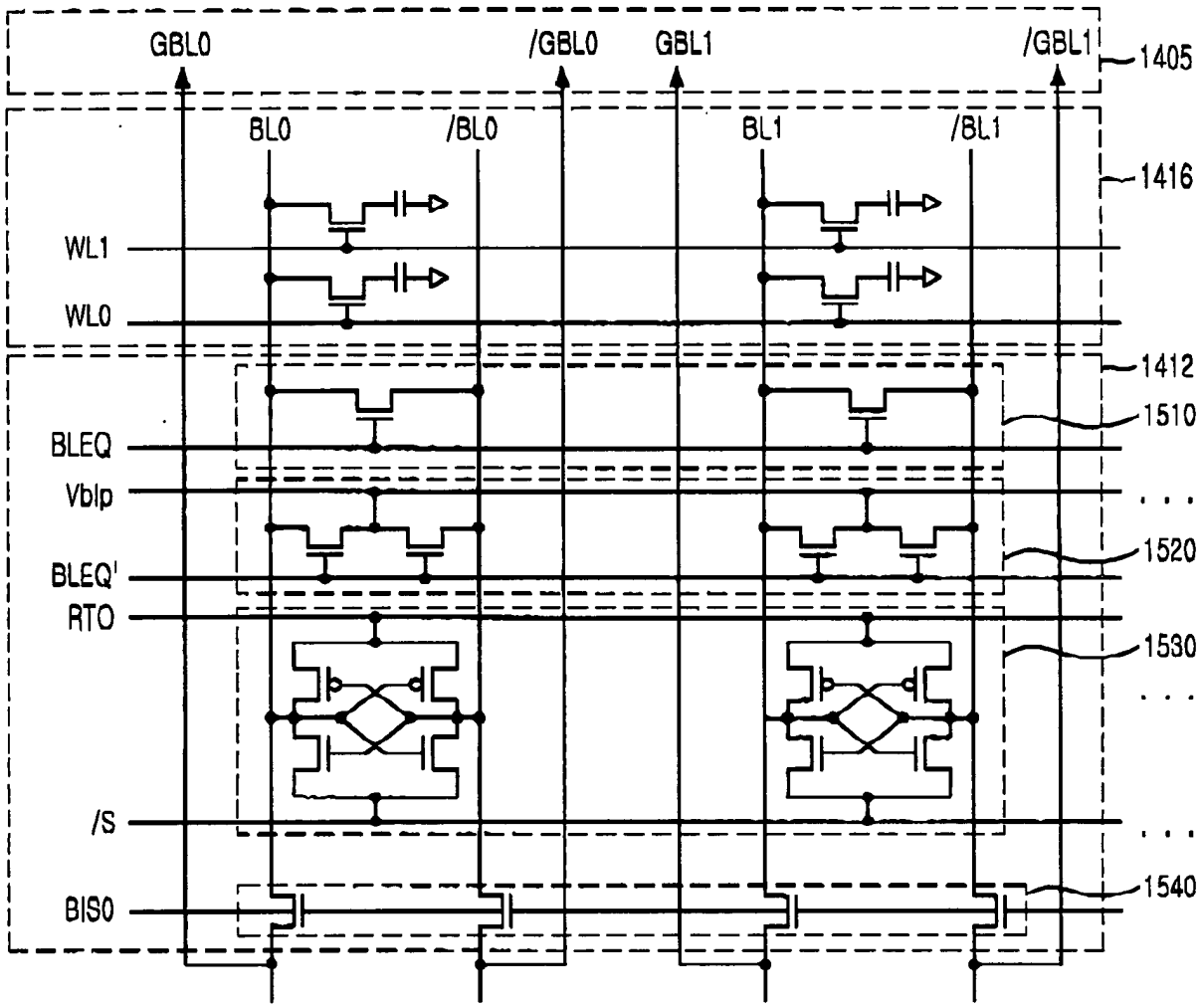

GBL0
/GBL0
GBL1
/GBL1
1405
BL0
/BL0
BL1
/BL1
1416
WL1
WL0
1412
1510
BLEQ
Vblp
1520
BLEQ'
RTO
1530
/S
1540
BIS0

FIG. 16

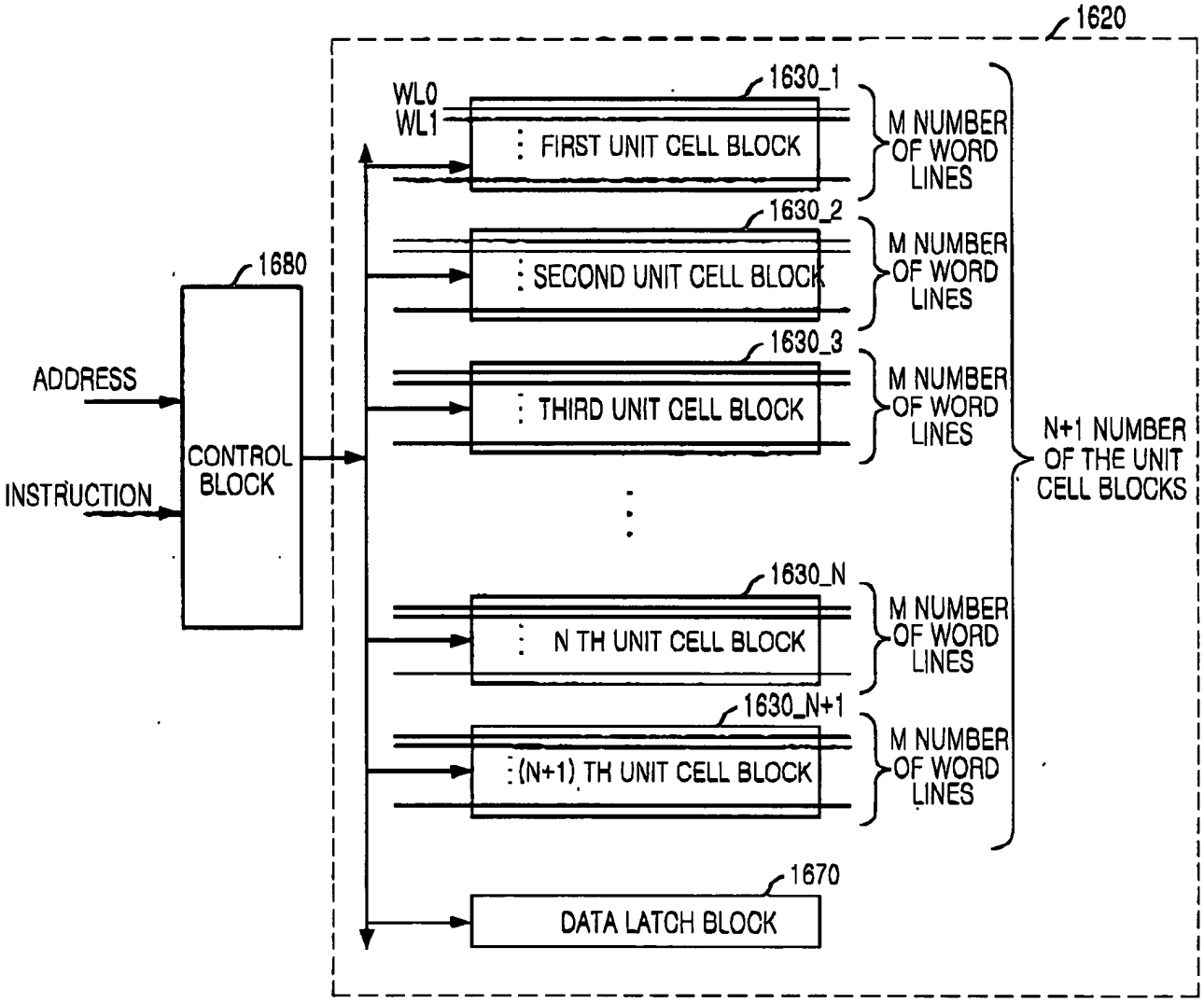

1620
1630_1
WL0
WL1
FIRST UNIT CELL BLOCK
M NUMBER OF WORD LINES
1630_2
SECOND UNIT CELL BLOCK
M NUMBER OF WORD LINES
1680
ADDRESS
1630_3
THIRD UNIT CELL BLOCK
M NUMBER OF WORD LINES
CONTROL BLOCK
INSTRUCTION
N+1 NUMBER OF THE UNIT CELL BLOCKS
1630_N
N TH UNIT CELL BLOCK
M NUMBER OF WORD LINES
1630_N+1
(N+1) TH UNIT CELL BLOCK
M NUMBER OF WORD LINES
1670
DATA LATCH BLOCK

FIG. 17

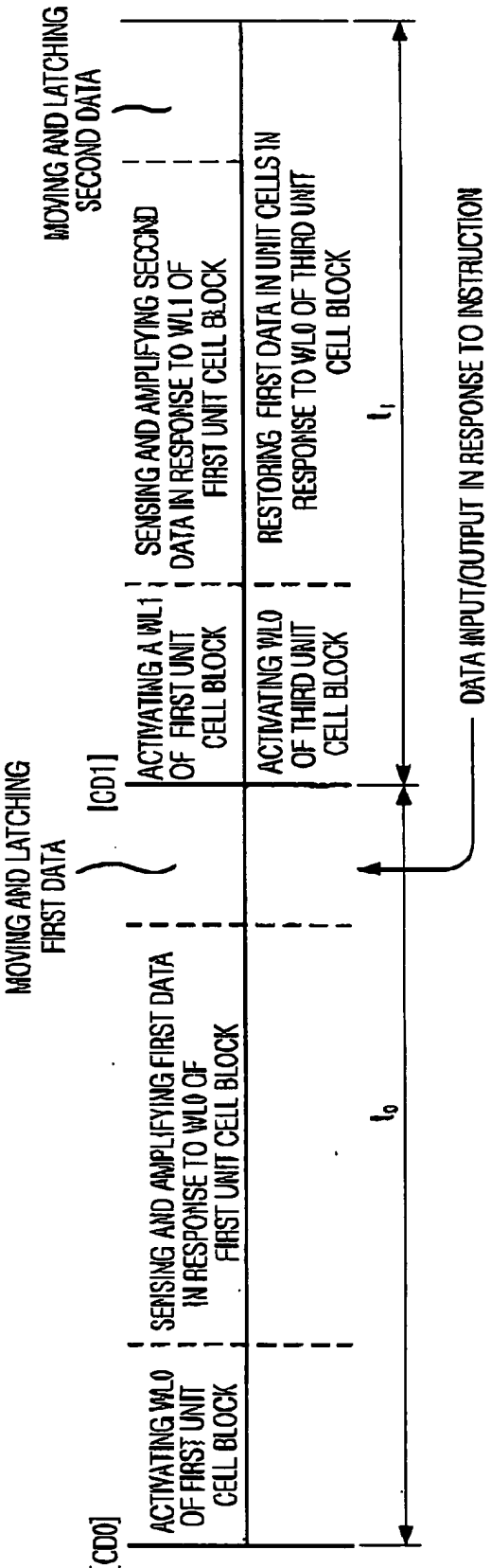

[CD0]
[CD1]
ACTIVATING WL0 OF FIRST UNIT CELL BLOCK
SENSING AND AMPLIFYING FIRST DATA IN RESPONSE TO WL0 OF FIRST UNIT CELL BLOCK
MOVING AND LATCHING FIRST DATA
ACTIVATING A WL1 OF FIRST UNIT CELL BLOCK
SENSING AND AMPLIFYING SECOND DATA IN RESPONSE TO WL1 OF FIRST UNIT CELL BLOCK
MOVING AND LATCHING SECOND DATA
ACTIVATING WL0 OF THIRD UNIT CELL BLOCK
RESTORING FIRST DATA IN UNIT CELLS IN RESPONSE TO WL0 OF THIRD UNIT CELL BLOCK
t_0
t_1
DATA INPUT/OUTPUT IN RESPONSE TO INSTRUCTION

FIG. 18

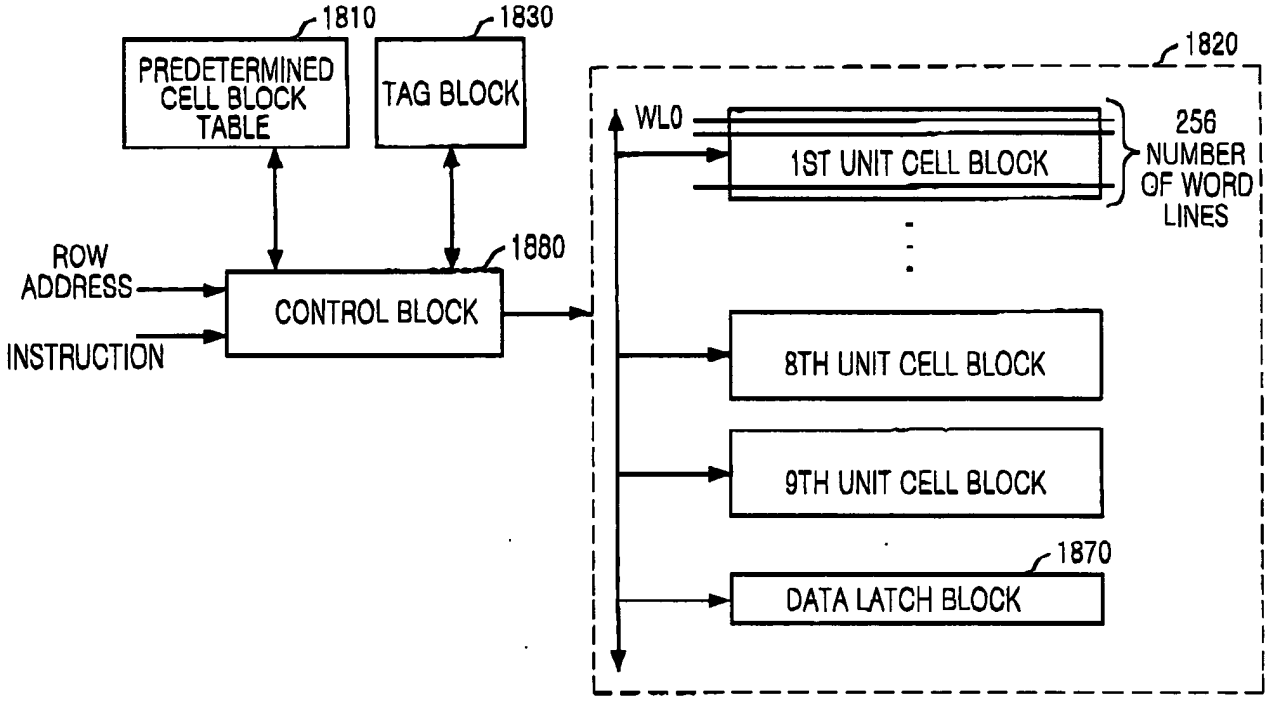

1810
PREDETERMINED CELL BLOCK TABLE
1830
TAG BLOCK
1820
WL0
1ST UNIT CELL BLOCK
256 NUMBER OF WORD LINES
ROW ADDRESS
1880
CONTROL BLOCK
INSTRUCTION
8TH UNIT CELL BLOCK
9TH UNIT CELL BLOCK
1870
DATA LATCH BLOCK

FIG. 19

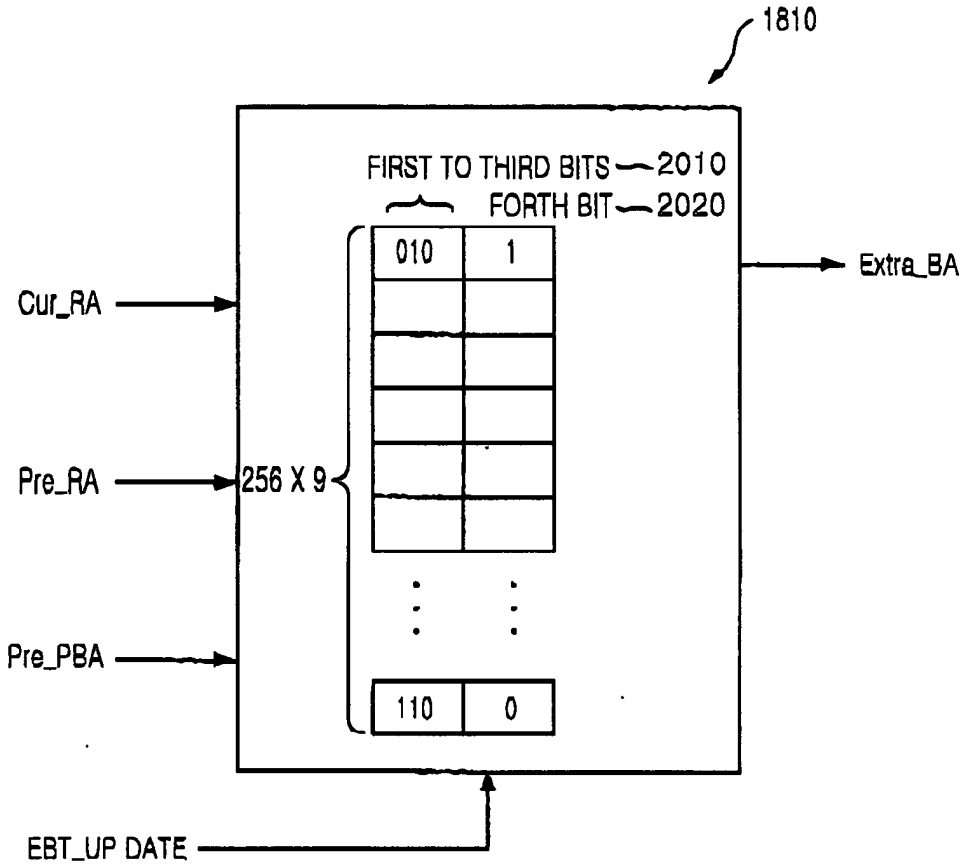

1810
FIRST TO THIRD BITS
2010
FORTH BIT
2020
010
1
110
0
256 X 9
Cur_RA
Pre_RA
Pre_PBA
EBT_UP DATE
Extra_BA

FIG. 20

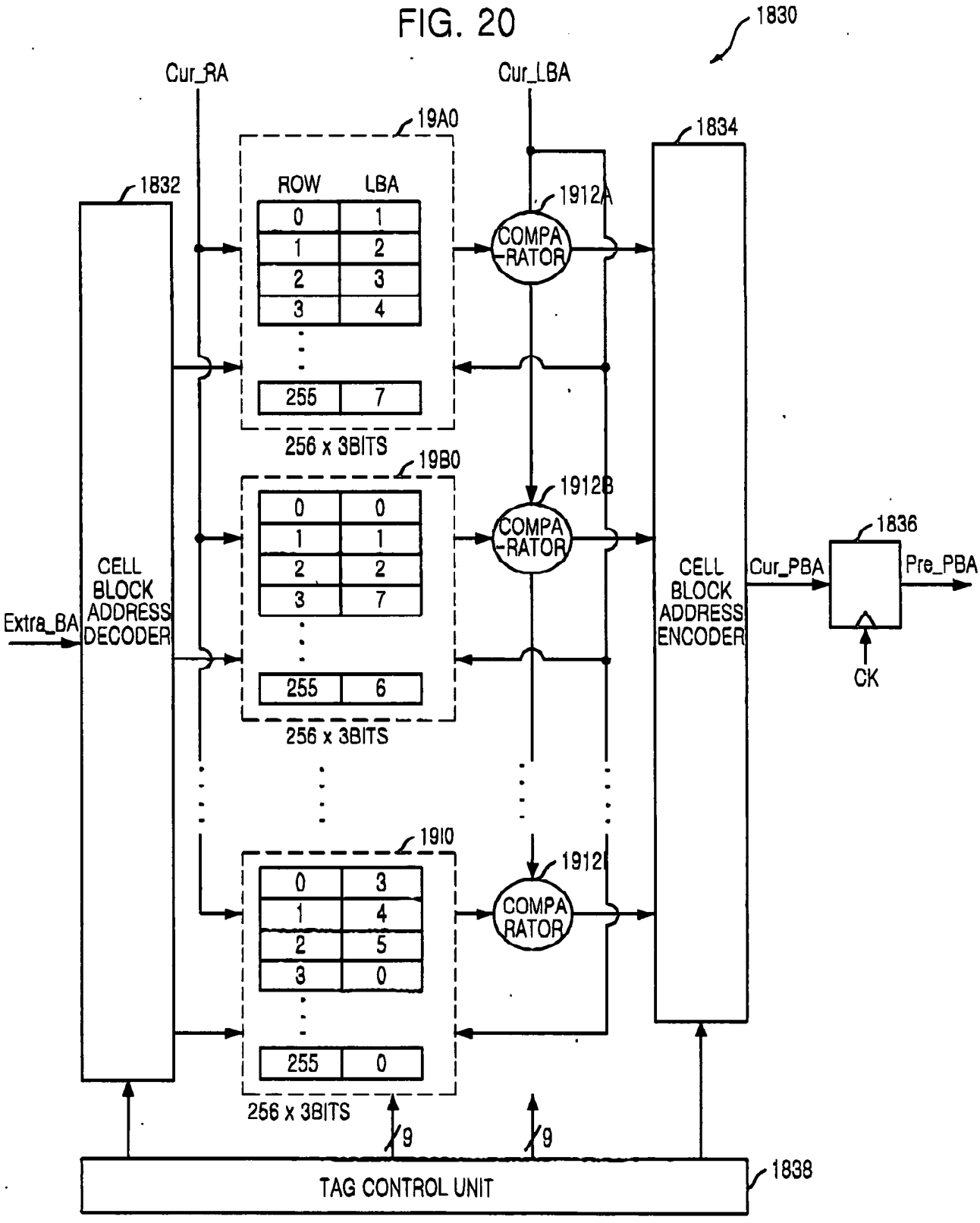

1830
Cur_RA
Cur_LBA
19A0
1834
1832
ROW
LBA
1912A
COMPA
-RATOR
0
1
1
2
2
3
3
4
255
7
256 x 3BITS
19B0
1912B
0
0
1
1
2
2
3
7
255
6
256 x 3BITS
1836
CELL
BLOCK
ADDRESS
DECODER
Extra_BA
CELL
BLOCK
ADDRESS
ENCODER
Cur_PBA
Pre_PBA
CK
1910
1912I
0
3
1
4
2
5
3
0
255
0
256 x 3BITS
9
9
TAG CONTROL UNIT
1838

FIG. 21

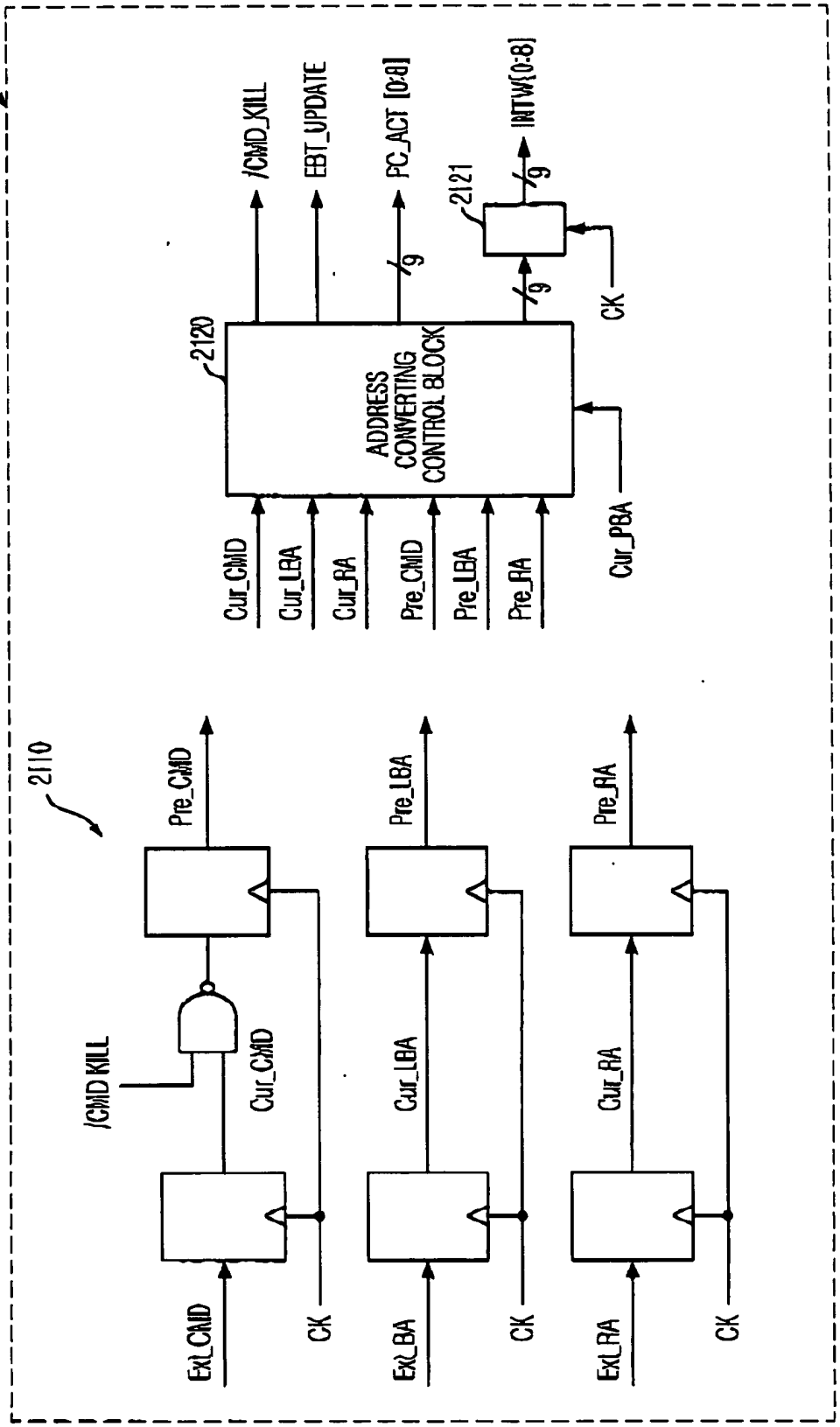

1880
2110
/CMD KILL
Cur_CMD
Pre_CMD
Ext_CMD
CK
Cur_LBA
Pre_LBA
Ext_BA
CK
Cur_RA
Pre_RA
Ext_RA
CK
2120
ADDRESS CONVERTING CONTROL BLOCK
Cur_CMD
Cur_LBA
Cur_RA
Pre_CMD
Pre_LBA
Pre_RA
Cur_PBA
/CMD_KILL
EBT_UPDATE
PC_ACT [0:8]
9
2121
INTW[0:8]
9
9
CK

FIG. 22

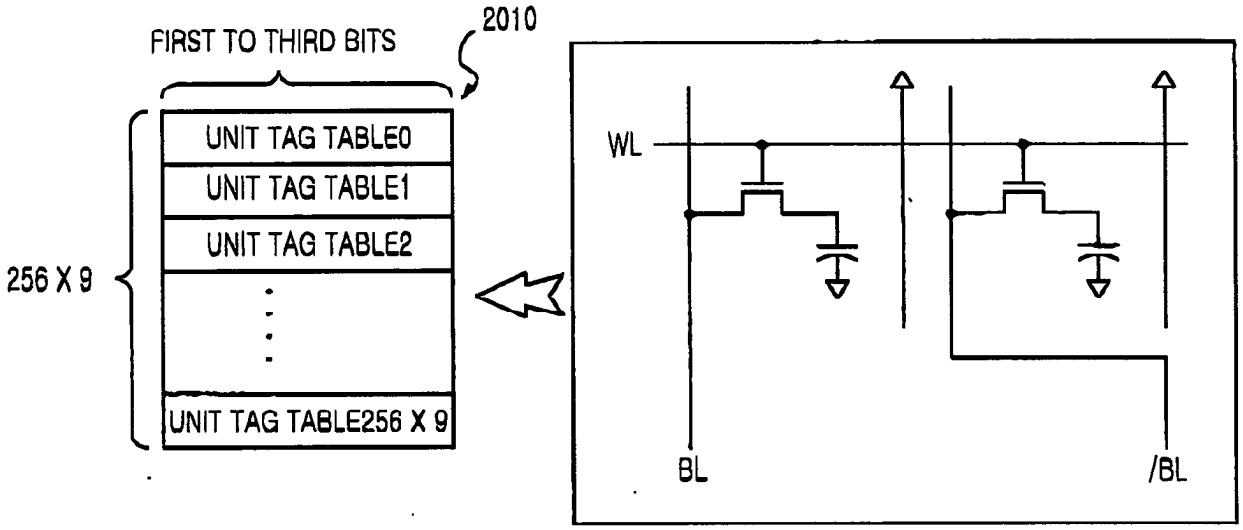

FIRST TO THIRD BITS
2010
UNIT TAG TABLE0
UNIT TAG TABLE1
UNIT TAG TABLE2
256 X 9
UNIT TAG TABLE256 X 9
WL
BL
/BL

FIG. 23

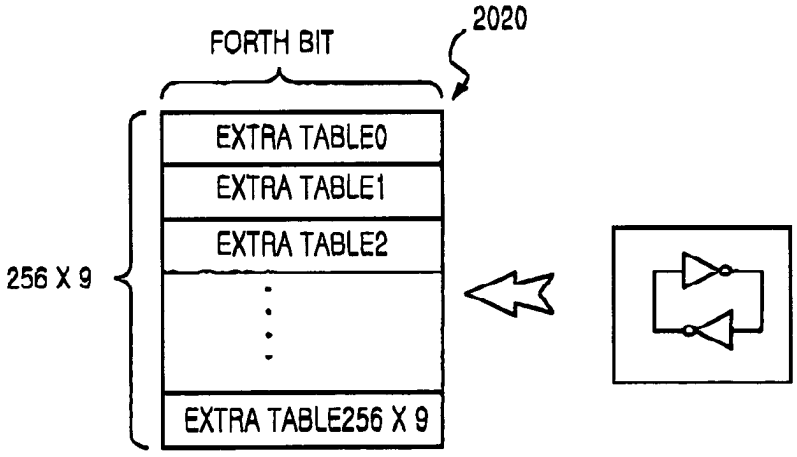

FORTH BIT
2020
EXTRA TABLE0
EXTRA TABLE1
EXTRA TABLE2
256 X 9
EXTRA TABLE256 X 9

FIG. 24

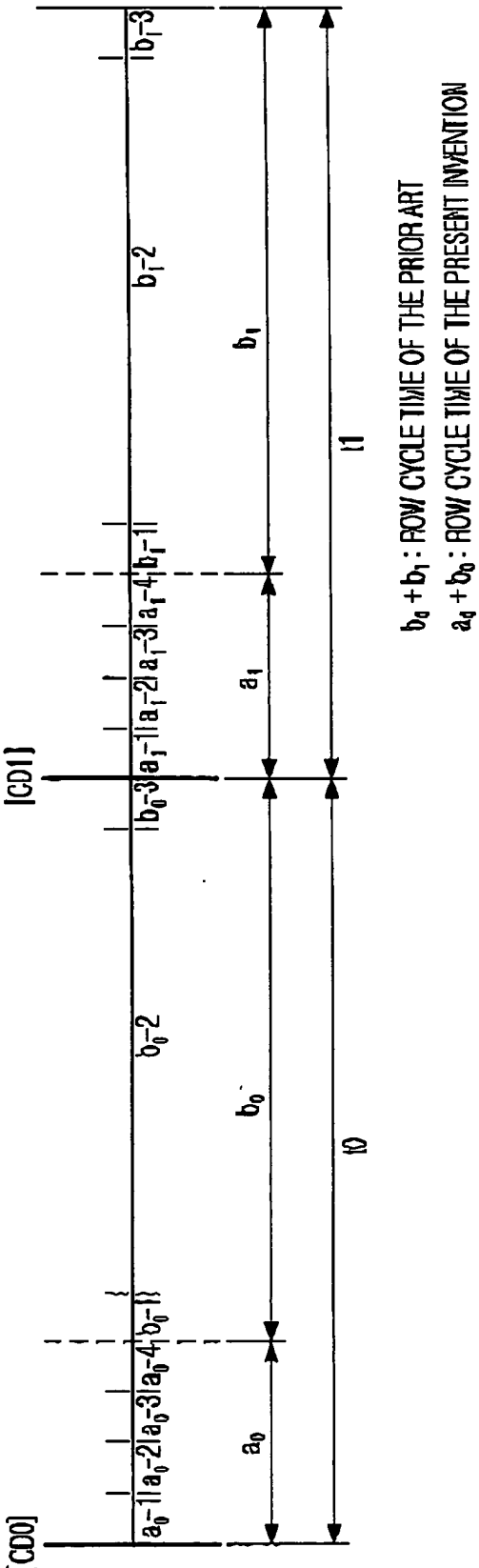
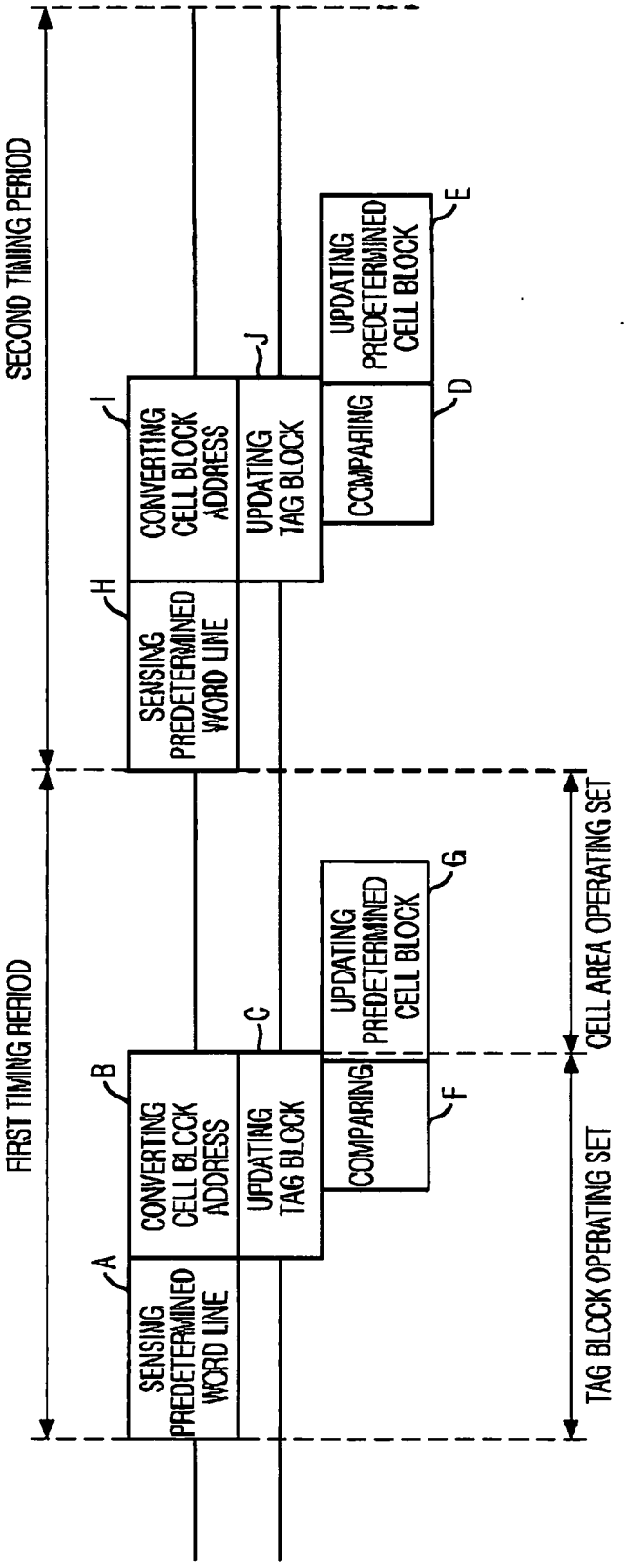

[CD0]
[CD1]
a_0-1 a_0-2 a_0-3 a_0-4 b_0-1
b_0-2
b_0-3 a_1-1 a_1-2 a_1-3 a_1-4 b_1-1
b_1-2
b_1-3
a_0
b_0
$t0$
a_1
b_1
$t1$
$b_0 + b_1$: ROW CYCLE TIME OF THE PRIOR ART
$a_1 + b_0$: ROW CYCLE TIME OF THE PRESENT INVENTION

FIG. 25


FIRST TIMING PERIOD
SECOND TIMING PERIOD
SENSING PREDETERMINED WORD LINE
CONVERTING CELL BLOCK ADDRESS
UPDATING TAG BLOCK
COMPARING
UPDATING PREDETERMINED CELL BLOCK
A
B
C
D
E
F
G
H
I
J
TAG BLOCK OPERATING SET
CELL AREA OPERATING SET

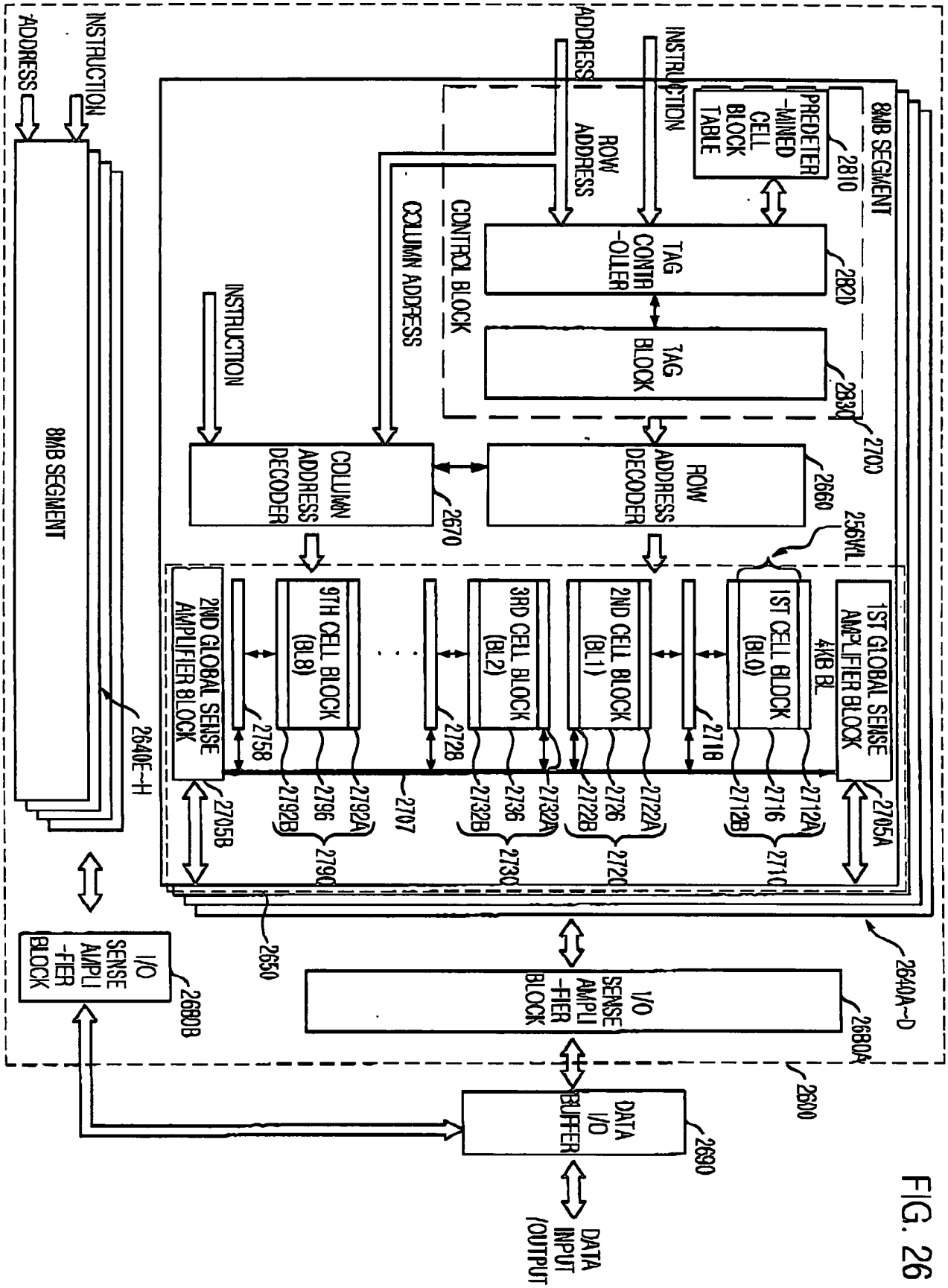

8MB SEGMENT
PREDETER-MINED CELL BLOCK TABLE
2810
TAG CONTR-OLLER
2820
TAG BLOCK
2830
2700
ROW ADDRESS
INSTRUCTION
CONTROL BLOCK
COLUMN ADDRESS
INSTRUCTION
ADDRESS
INSTRUCTION
COLUMN ADDRESS DECODER
2670
ROW ADDRESS DECODER
2660
256KB
1ST GLOBAL SENSE AMPLIFIER BLOCK
4KB BL
1ST CELL BLOCK (BL0)
2ND CELL BLOCK (BL1)
3RD CELL BLOCK (BL2)
9TH CELL BLOCK (BL8)
2ND GLOBAL SENSE AMPLIFIER BLOCK
2705A
2712A
2712B
2716
2718
2722A
2722B
2726
2728
2732A
2732B
2736
2758
2792A
2792B
2796
2705B
2707
2710
2720
2730
2790
2640A~D
2640E~H
8MB SEGMENT
2650
I/O SENSE AMPLI-FIER BLOCK
2680A
2680B
2600
DATA I/O BUFFER
2690
DATA INPUT /OUTPUT

FIG. 26

FIG. 27

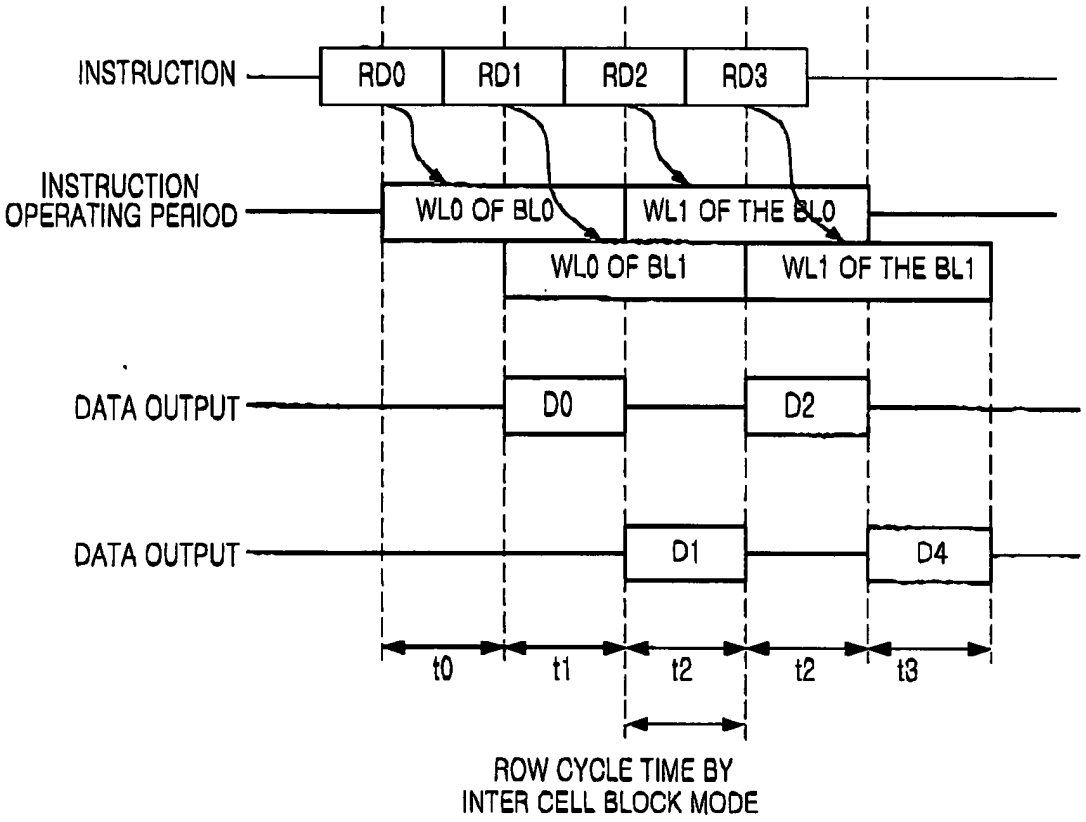

INSTRUCTION
RD0
RD1
RD2
RD3
INSTRUCTION OPERATING PERIOD
WL0 OF BL0
WL1 OF THE BL0
WL0 OF BL1
WL1 OF THE BL1
DATA OUTPUT
D0
D2
DATA OUTPUT
D1
D4
t0
t1
t2
t2
t3
ROW CYCLE TIME BY INTER CELL BLOCK MODE

FIG. 28

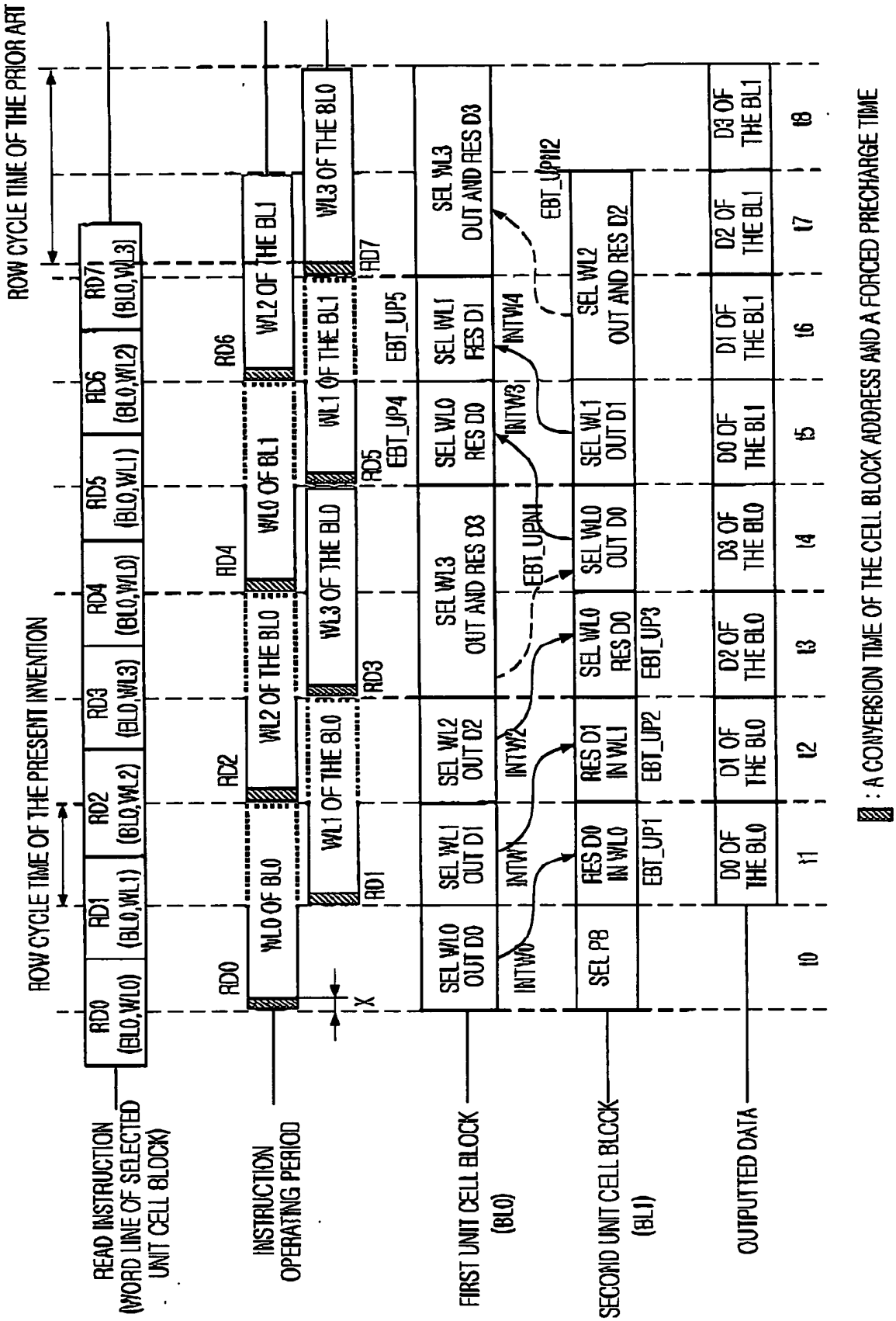

ROW CYCLE TIME OF THE PRIOR ART
ROW CYCLE TIME OF THE PRESENT INVENTION
READ INSTRUCTION (WORD LINE OF SELECTED UNIT CELL BLOCK)
INSTRUCTION OPERATING PERIOD
FIRST UNIT CELL BLOCK (BL0)
SECOND UNIT CELL BLOCK (BL1)
OUTPUTTED DATA
RD0 (BL0,WL0)
RD1 (BL0,WL1)
RD2 (BL0,WL2)
RD3 (BL0,WL3)
RD4 (BL1,WL0)
RD5 (BL1,WL1)
RD6 (BL1,WL2)
RD7 (BL1,WL3)
WL0 OF BL0
WL1 OF THE BL0
WL2 OF THE BL0
WL3 OF THE BL0
WL0 OF BL1
WL1 OF THE BL1
WL2 OF THE BL1
WL3 OF THE BL0
X
SEL WL0 OUT D0
SEL WL1 OUT D1
SEL WL2 OUT D2
SEL WL3 OUT AND RES D3
SEL WL0 RES D0
SEL WL1 RES D1
SEL WL3 OUT AND RES D3
INTW0
INTW1
INTW2
INTW3
INTW4
EBT_UP1
EBT_UP2
EBT_UP3
EBT_UP4
EBT_UP5
EBT_UP12
SEL PB
RES D0 IN WL0
RES D1 IN WL1
SEL WL0 RES D0
SEL WL0 OUT D0
SEL WL1 OUT D1
SEL WL2 OUT AND RES D2
D0 OF THE BL0
D1 OF THE BL0
D2 OF THE BL0
D3 OF THE BL0
D0 OF THE BL1
D1 OF THE BL1
D2 OF THE BL1
D3 OF THE BL1
t0
t1
t2
t3
t4
t5
t6
t7
t8
: A CONVERSION TIME OF THE CELL BLOCK ADDRESS AND A FORCED PRECHARGE TIME

FIG. 29

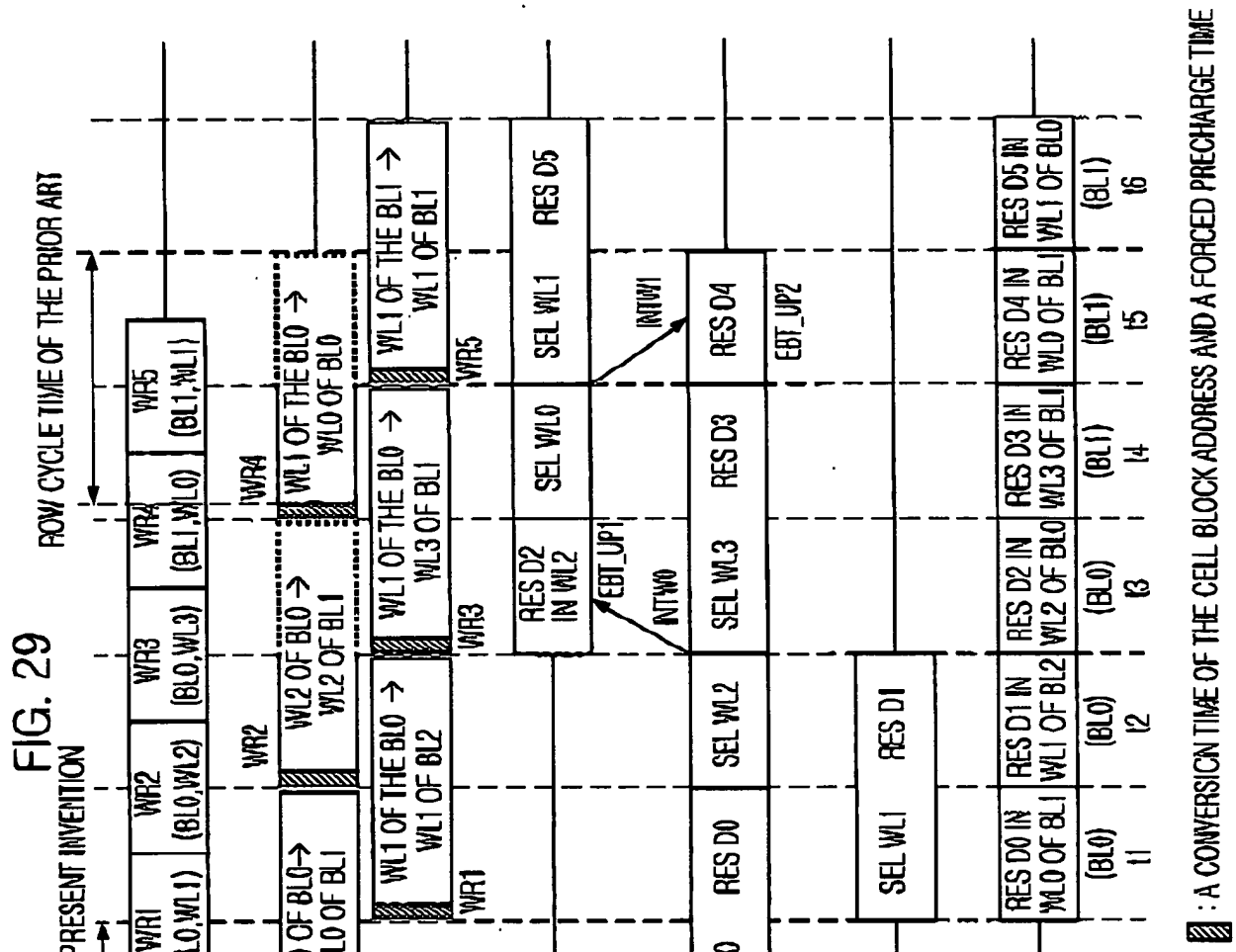

ROW CYCLE TIME OF THE PRESENT INVENTION
ROW CYCLE TIME OF THE PRIOR ART
READ INSTRUCTION (LOGICAL CELL BLOCK ADDRESS)
INSTRUCTION OPERATING PERIOD (CHANGE THE LOGICAL CELL ADDRESS TO PHYSICAL CELL BLOCK ADDRESS)
FIRST UNIT CELL BLOCK (BL0)
SECOND UNIT CELL BLOCK (BL1)
THIRD UNIT CELL BLOCK (BL2)
UNIT CELL BLOCK STORING DATA (THE LOGICAL CELL BLOCK ADDRESS)
WR0 (BL0,WL0)
WR1 (BL0,WL1)
WR2 (BL0,WL2)
WR3 (BL0,WL3)
WR4 (BL1,WL0)
WR5 (BL1,WL1)
WL0 OF BL0→ WL0 OF BL1
WL2 OF BL0→ WL2 OF BL1
WL0 OF THE BL1→ WL0 OF BL0
WL1 OF THE BL0→ WL1 OF BL2
WL3 OF BL0→ WL3 OF BL1
WL1 OF THE BL1→ WL1 OF BL1
RES D2 IN WL2
SEL WL0
SEL WL1
RES D5
EBT_UP1
INTW0
INTW1
SEL WL0
RES D0
SEL WL2
SEL WL3
RES D3
RES D4
EBT_UP2
SEL WL1
RES D1
RES D0 IN WL0 OF BL1
RES D1 IN WL1 OF BL2
RES D2 IN WL2 OF BL0
RES D3 IN WL3 OF BL1
RES D4 IN WL0 OF BL1
RES D5 IN WL1 OF BL0
10
11
12
13
14
15
16
: A CONVERSION TIME OF THE CELL BLOCK ADDRESS AND A FORCED PRECHARGE TIME

FIG. 30

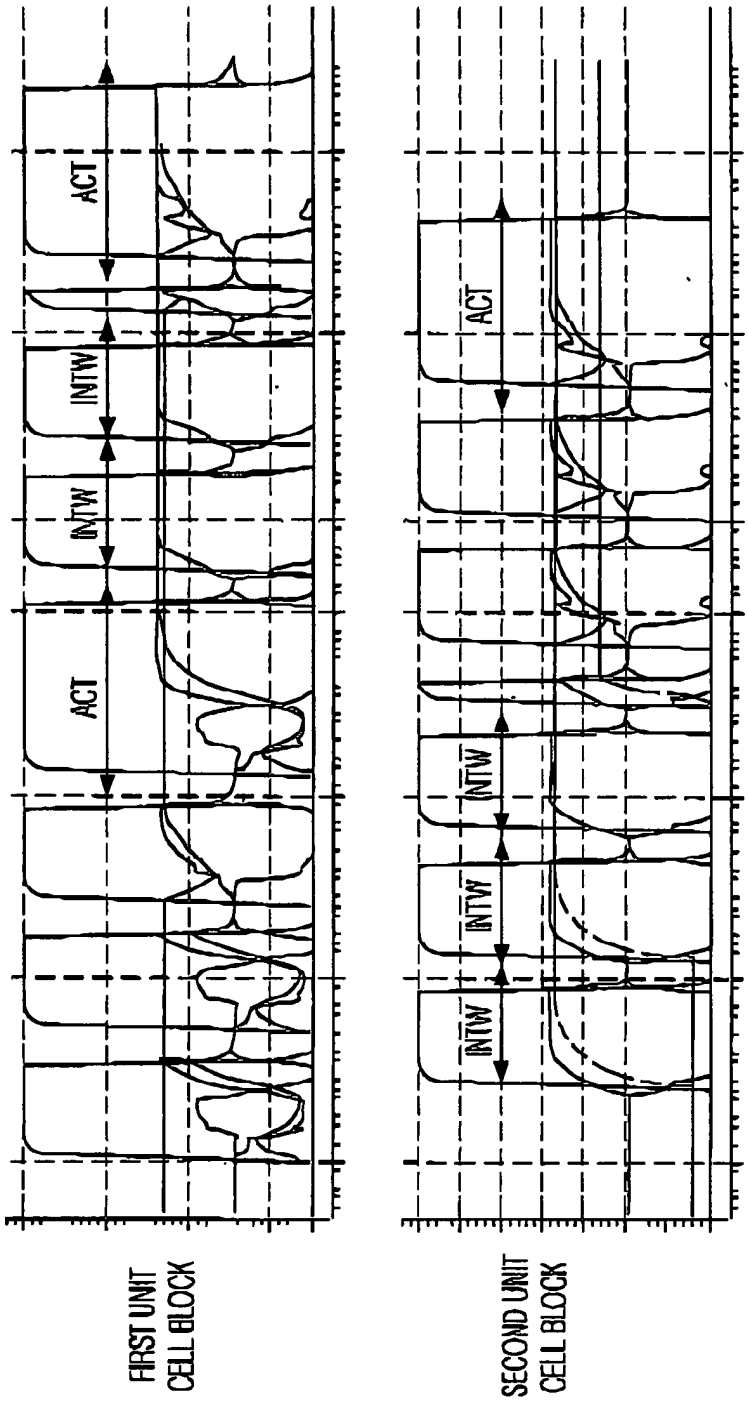

ACT
INTW
INTW
ACT
FIRST UNIT CELL BLOCK
ACT
INTW
INTW
INTW
SECOND UNIT CELL BLOCK

FIG. 31

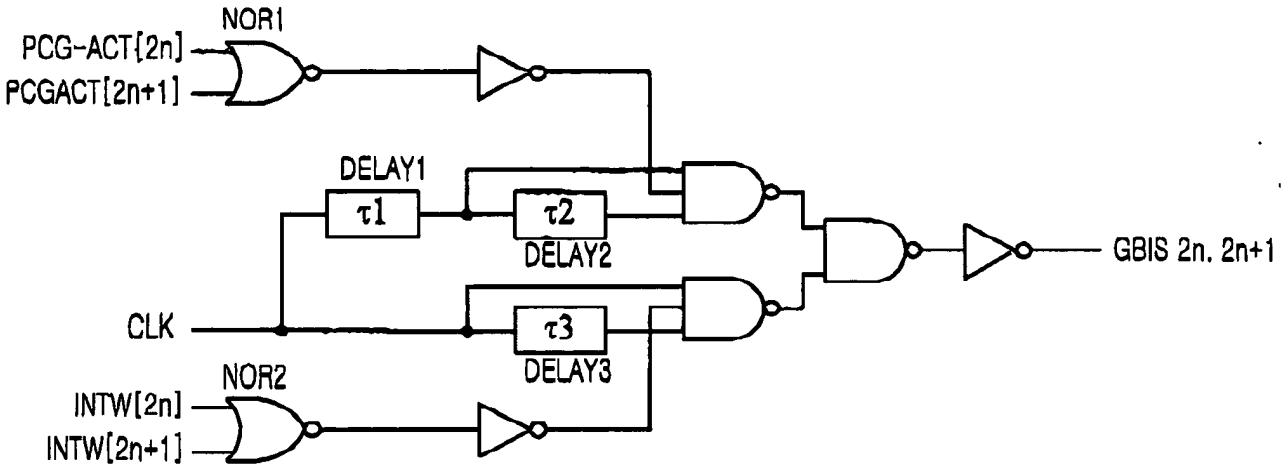

NOR1
PCG-ACT[2n]
PCGACT[2n+1]
DELAY1
τ1
τ2
DELAY2
CLK
τ3
DELAY3
NOR2
INTW[2n]
INTW[2n+1]
GBIS 2n, 2n+1

FIG. 32

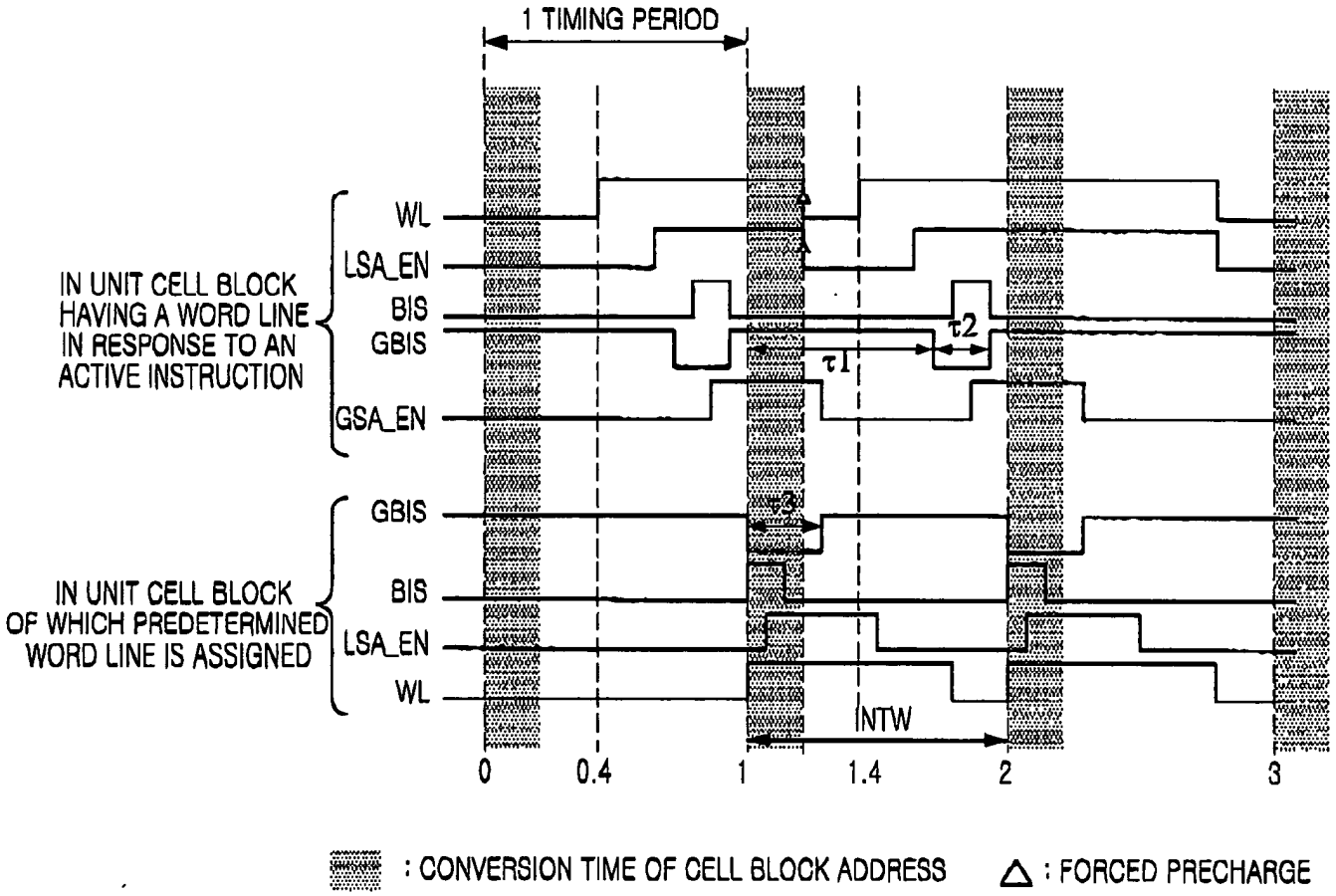

1 TIMING PERIOD
IN UNIT CELL BLOCK HAVING A WORD LINE IN RESPONSE TO AN ACTIVE INSTRUCTION
WL
LSA_EN
BIS
GBIS
GSA_EN
τ1
τ2
IN UNIT CELL BLOCK OF WHICH PREDETERMINED WORD LINE IS ASSIGNED
GBIS
BIS
LSA_EN
WL
τ3
tNTW
0
0.4
1
1.4
2
3
: CONVERSION TIME OF CELL BLOCK ADDRESS
△ : FORCED PRECHARGE

FIG. 33

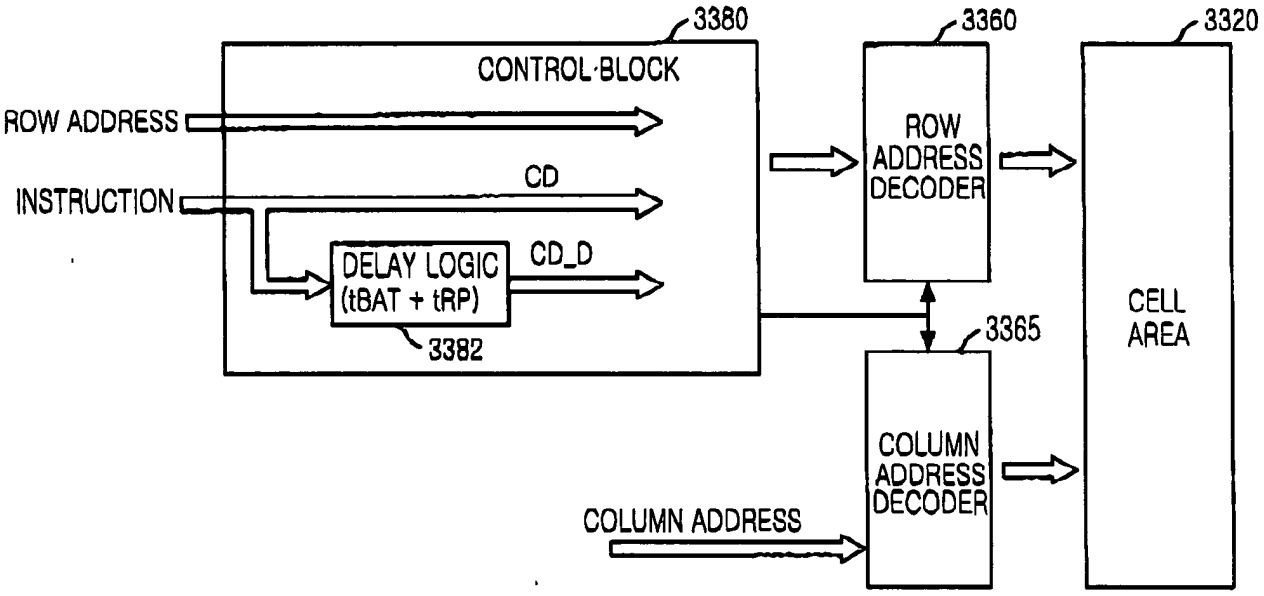

3380
CONTROL BLOCK
ROW ADDRESS
INSTRUCTION
CD
DELAY LOGIC
(tBAT + tRP)
CD_D
3382
3360
ROW
ADDRESS
DECODER
3320
CELL
AREA
3365
COLUMN
ADDRESS
DECODER
COLUMN ADDRESS

FIG. 34

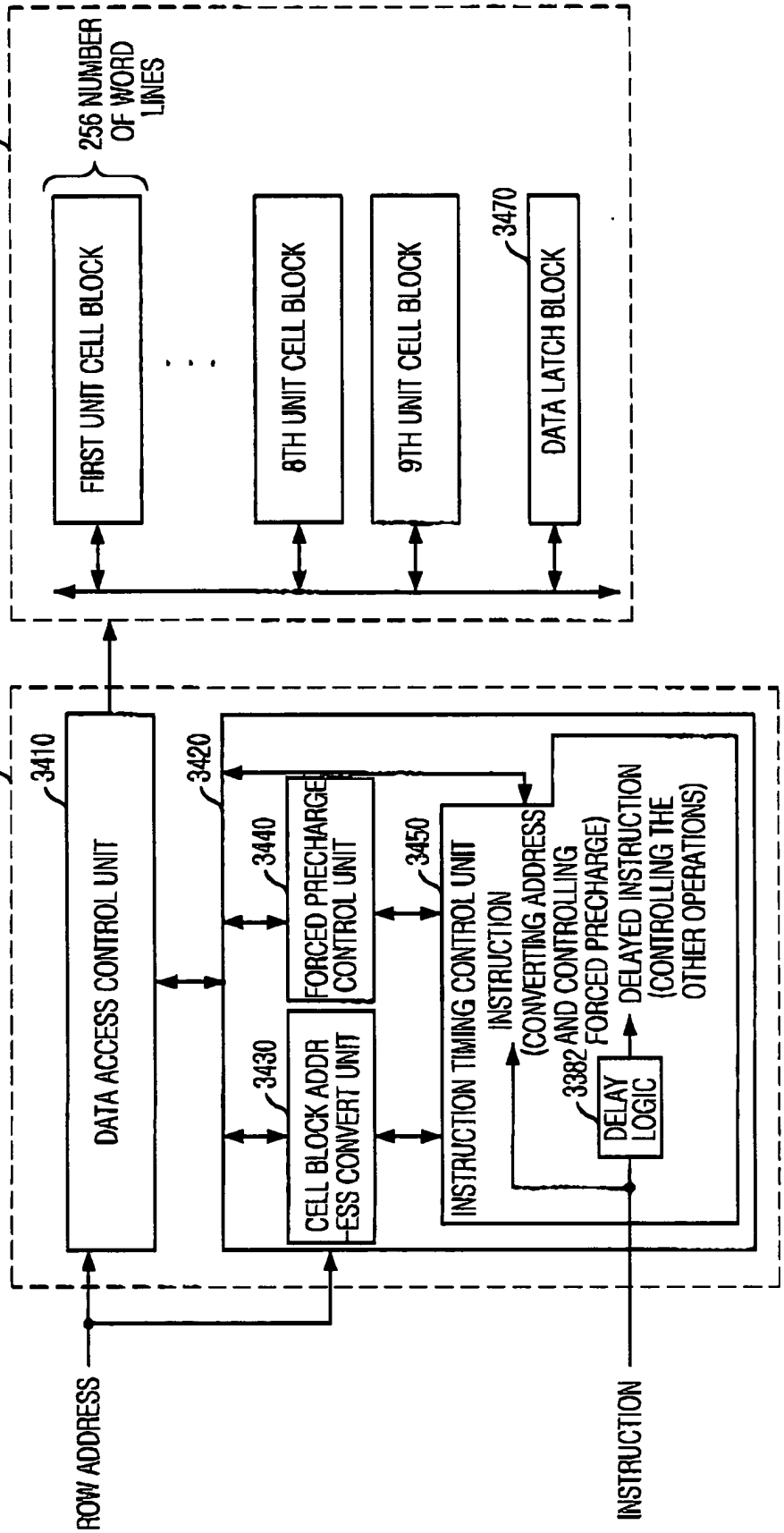

3320
256 NUMBER OF WORD LINES
FIRST UNIT CELL BLOCK
8TH UNIT CELL BLOCK
9TH UNIT CELL BLOCK
3470
DATA LATCH BLOCK
3380
3410
DATA ACCESS CONTROL UNIT
3420
3440
FORCED PRECHARGE CONTROL UNIT
3450
INSTRUCTION TIMING CONTROL UNIT
INSTRUCTION (CONVERTING ADDRESS AND CONTROLLING FORCED PRECHARGE)
3382
DELAY LOGIC
DELAYED INSTRUCTION (CONTROLLING THE OTHER OPERATIONS)
3430
CELL BLOCK ADDRESS CONVERT UNIT
ROW ADDRESS
INSTRUCTION

FIG. 35

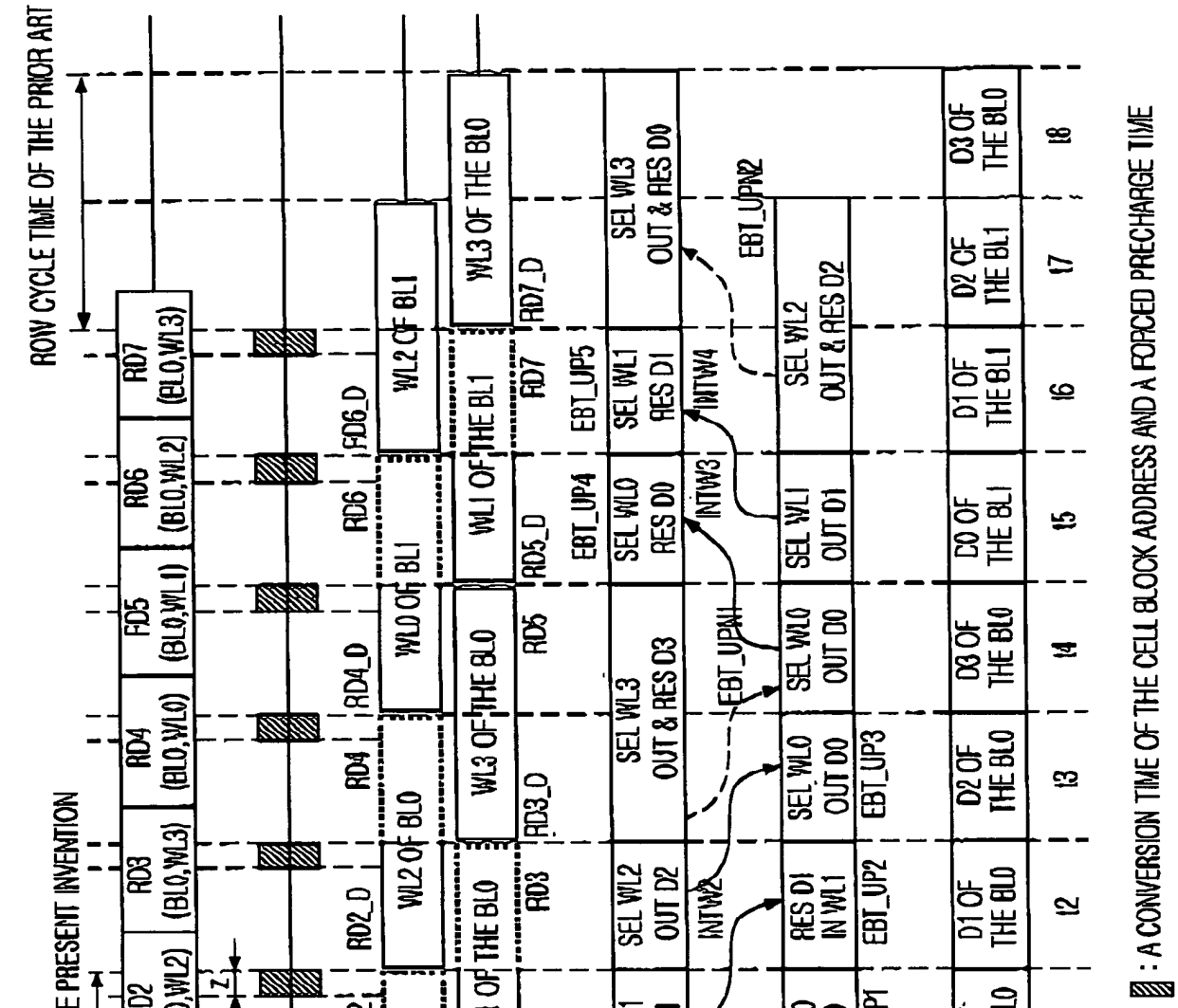
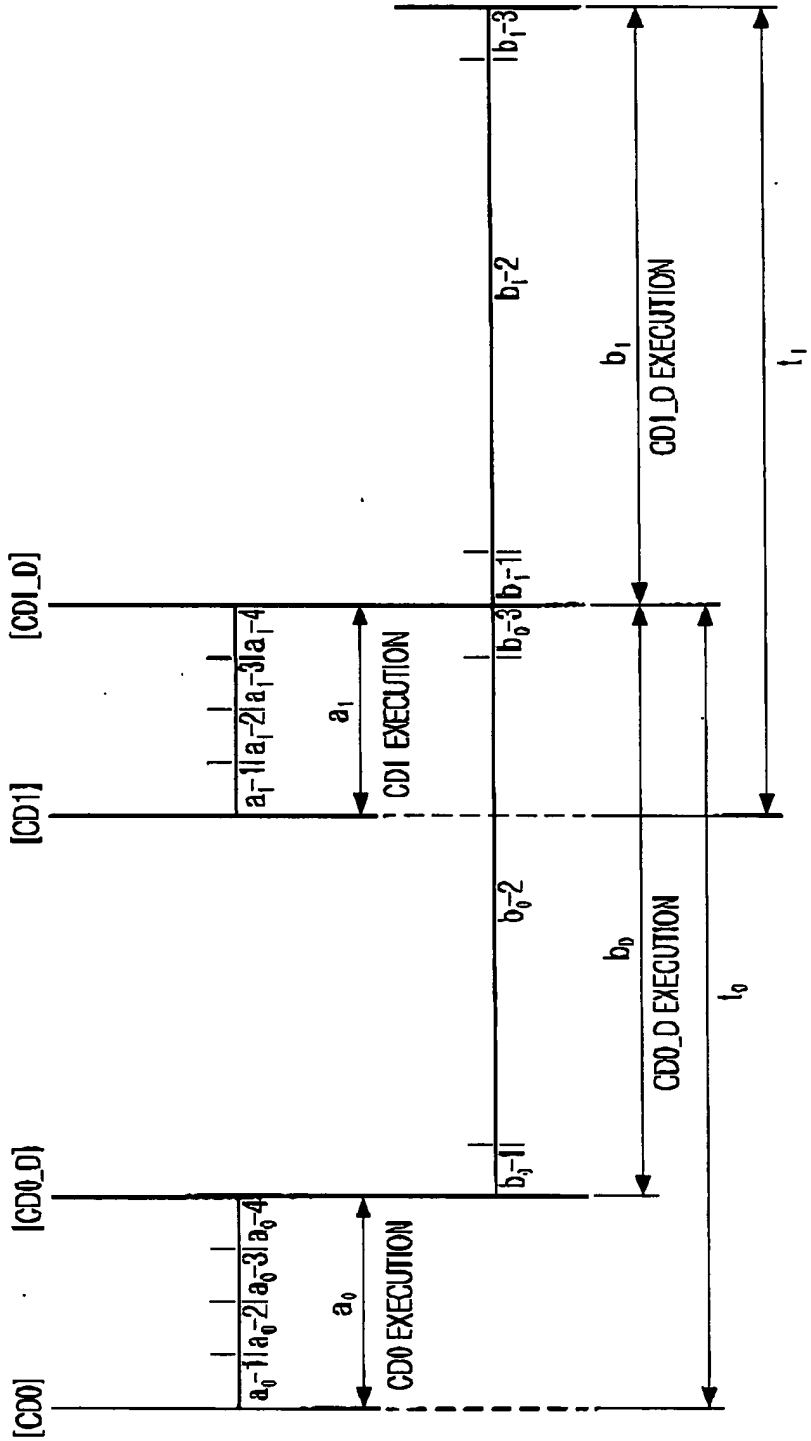

ROW CYCLE TIME OF THE PRIOR ART
ROW CYCLE TIME OF THE PRESENT INVENTION
READ INSTRUCTION (LOGICAL CELL BLOCK ADDRESS)
A CONVERSION TIME OF THE CELL BLOCK ADDRESS AND A FORCED PRECHARGE TIME
INSTRUCTION OPERATING PERIOD
FIRST UNIT CELL BLOCK
SECOND UNIT CELL BLOCK
OUTPUTTED DATA
RD0 (BL0,WL0)
RD1 (BL0,WL1)
RD2 (BL0,WL2)
RD3 (BL0,WL3)
RD4 (BL0,WL0)
RD5 (BL0,WL1)
RD6 (BL0,WL2)
RD7 (BL0,WL3)
RD0_D
RD1_D
RD2_D
RD3_D
RD4_D
RD5_D
RD6_D
RD7_D
WL0 OF BL0
WL1 OF THE BL0
WL2 OF BL0
WL3 OF THE BL0
WL0 OF BL1
WL1 OF THE BL1
WL2 OF BL1
WL3 OF THE BL0
EBT_UP1
EBT_UP2
EBT_UP3
EBT_UP4
EBT_UP5
EBT_UPW1
EBT_UPW2
INTW1
INTW2
INTW3
INTW4
SEL WL0 OUT D0
SEL WL1 OUT D1
SEL WL2 OUT D2
SEL WL3 OUT & RES D3
SEL WL0 RES D0
SEL WL1 RES D1
SEL WL2 OUT & RES D2
SEL WL3 OUT & RES D0
SEL_PB
RES D0 IN WL0
RES D1 IN WL1
SEL WL0 OUT D0
SEL WL1 OUT D1
D0 OF THE BL0
D1 OF THE BL0
D2 OF THE BL0
D3 OF THE BL0
D0 OF THE BL1
D1 OF THE BL1
D2 OF THE BL1
D3 OF THE BL0
t0
t1
t2
t3
t4
t5
t6
t7
t8
x
y
z
: A CONVERSION TIME OF THE CELL BLOCK ADDRESS AND A FORCED PRECHARGE TIME

FIG. 36


[CD0]
[CD0_D]
[CD1]
[CD1_D]
a_0-1 a_0-2 a_0-3 a_0-4
a_0
CD0 EXECUTION
a_1-1 a_1-2 a_1-3 a_1-4
a_1
CD1 EXECUTION
b_0-1
b_0-2
b_0
CD0_D EXECUTION
t_0
b_1-1
b_1-2
b_1-3
b_1
CD1_D EXECUTION
t_1
$b_0 + b_1$ (tRC) : ROW CYCLE TIME OF THE PRIOR ART
b_0 1/2(tRC) : ROW CYCLE TIME OF THE PRESENT INVENTION